

Skylake-LP/H - Intel[®] Management Engine Firmware 11.0

Corporate Firmware Bring Up Guide

June 2015

Revision 1.033 - Beta 2 Release

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Revision	Description	Date
11.0.0.1080	Pre-Alpha Release: See change bars on the left side of the page.	September 2014
11.0.0.1100	Alpha Release: See change bars on the left side of the page.	December 2014
11.0.0.1106	ICC table additions: See change bars on the left side of the page.	January 2015
11.0.0.11xx	General table additions: See change bars on the left side of the page for specific page change.	February 2015
	 Updated Table of Contents, List of Figures, and List of Tables to align with table content shifts for added items 	
	Page 28 - Updated screen shot to reflect tool update	
	Page 40, 41 added missing table values	
	 Page 50 - Removed frequency values that were not valid 	
	Page 78 - 89 - Table contents were shifted to allow for table additions	
	Page 94 - Help text was added for CPU strap settings	
11.0.0.11xx	Updates made to reflect changes in ME kit package contents in Chapter 1 and visual changes in CPU Strap section in Chapter 2.	March 2015
11.0.0.1122	Beta Release: Table updates made, see change bars on left side of the page for location	March 2015
	 Updated Table of Contents, List of Figures, and List of Tables to align with table content shifts for added items 	
	Appendix D - PTT table updated to ensure correct values	
	Added additional row to include region order in the build settings popup	
	Inserted EcRegion in Flash Layout section	
	Inserted EC Master Access in Flash Settings section	
	Inserted Post Manufacturing Lock to ME Kernel section	
	 Intel® AMT Watchdog Automatic Reset Enabled added to screen shot and table under Intel® AMT section under Intel® AMT Configuration 	
	Minimum removed as a choice for redirection privacy / security level	
	 Inserted screen shot and table for Hash Key Configuration for Bootguard /ISH and removed OEM Public Key Hash from Boot Guard Configuration under Platform Protection section 	
	Updated screen shot for USB3 Port Configuration under Flex I/O section	
	Added additional note for PCIe controllers for RST under Flex I/O section	
	 Updated screen shots to show removal of USB_Wakeout#/GPD7 signal configuration from GPIO and Power sections 	
	Updated ME Feature Pins under GPIO to reflect changes in UI layout	
	Removed Appendix E RVP CRB A Step configuration settings	
	Added Appendix after renumbering for ISH Public Key Information	
	 Updated WLAN Microcode version for Snowfield Peak in Networking and Connectivity Section 	
	 Updated CPU Straps section to IMON disabled = 0x1 	



Revision	Description	Date
11.0.0.1126	General Updates: Table updates made, see change bars on left side of the page for location	April 2015
	 Updated Table of Contents, List of Figures, and List of Tables to align with table content shifts for added items 	
	Updated kit content reference for BIOS and LAN version	
	 ICC Table 2.8 settings - Remove SPT-H only enable option reference for CLKRUN LPC 0 and CLKRUN LPC 1 	
	 ICC Table 2.8 removed options for SKL-U and SKL-Y GPIO settings that were not listed 	
	 Flash Settings > Flash Configuration changed screen shot to match fields displayed 	
	 Internal PCH Buses > PCH Timer Configuration - Added APWROK Timing back to table and updated screen shot 	
	 Debug > Intel® Trace Hub Technology - Added Unlock Token field to table and updated screen shot 	
	 Appendix B tables updated to differentiate between SPT-LP and SPT-H PCH configurations 	
	Appendix F references added	
	 Quad Output Read Enabled and Dual Output Read Enabled values changed. 	
	 Debug Override bit value tables added to description for pre-production and production silicon. 	
	 MCTPDevPortEC setting changed to value 0x02 and screen shot changed. 	
	Change BSP setting to disabled under Boot Guard Configuration.	
	 ICC Table 2.8 settings updated to reflect clock gating wait value changes, crystal oscillator description changes, and GPIO Pin Mappings. See change bar for specific locations. 	
	Screen shots changed for added fields	



Revision	Description	Date
11.0.0.1133	General Updates: Checked kit for updates to user interface	May 2015
	 Updated BSP Initialization description in table 2-7 Boot Guard Configuration 	
	 Updated Flash Settings section, write and erase clock frequency to 48MHz 	
	Updated Flex I/O Section, SKL-H column to match default settings	
11.0.0.1136	General Updates: Checked kit for updates to user interface	May 2015
	 Updated Platform Protection > Content Protection screen shot and added associated new rows to table 2-7 section 1 	
	Added IDLM under Debug table 2-15 section 4 with screen shot	
11.0.0.1144	General Updates: Checked kit for updates to user interface	June 2015
	 Updated Platform Protection > Content Protection screen shot and added associated new rows to table 2-7 section 1 	
	Updated master pages to resolve numbering issue	
	 Removed conditional indicators from template for previous platforms and cleaned up document to only include corporate/consumer indicators 	
	 Changed table format to allow for future formatting to easier add Lewisburg features 	
	 Added Intel® Network Frame Forwarder section in Intel® ME Kernel section and reordered remaining graphics and numbers accordingly 	
	Changed DCI Enabled to Yes	
	Debug Override Pre-Production Silicon Bit 0: timeout changed to 60	
	 HDCP Internal Display Port1 – 5K changed to none 	
	 Moved Note in content protection section to each HDCP section and made conditional to corporate 	
	Flex I/O port settings updated for inconsistencies	
	BSP settings changed to enabled	
	MctpDevicePortEc set to 0x0	
	 Flash Settings Invalid Instructions changed to match current settings and internal sighting 225442 	
	 Internal sighting 225139 - SataPCIeComboPort1 should be GPIO instead PCIe (or GbE) on RVP3 	
	Updated screen shot for PCH Timer Configuration	
	Internal sighting 5253614 - SKL-H USB3/PCIe Combo Port Mapping Typo	
	GT US Power Plane Topology updated for setting mismatch	
	 Added general note to NFF section about some PCH not supporting enabling of this option 	
	Updated screen shot for ME region that included added display fields for Chipset Initialization	
	 Update eSPI CRC Check Enabled settings to match SPI programming guide values 	



1 Introduction

This document covers the Intel[®] Management Engine Firmware (Intel[®] ME) 11.0 - Corporate Firmware bring up procedure. Intel[®] ME is tied to essential platform functionality — this dependency cannot be avoided for engineering reasons.

The bring up procedure primarily involves building a Serial Peripheral Interface (SPI) Flash image that will contain:

- [required] Descriptor region Contains sizing information for all other SPI Flash image regions, SPI settings (including Vendor Specific Configuration or VSCC tables, SPI device parameters), and region access permissions.
- [required] BIOS region Contains firmware for the processor (or host) and/or Embedded Controller (EC).
- [required] Intel[®] ME FW region Contains firmware for the Intel[®] Management Engine.
- **[optional]** GbE region Contains firmware for Intel LAN solution.

For more details on SPI Flash layout, see the document **Skylake-LP/H SPI Programming Guide** and Appendix A. Once the SPI Flash image is built, it will be programmed to the target based platform and the platform will be booted. This document also covers any tests and checks required to ensure that this boot process is successful and that Intel[®] ME Corporate FW is operating as expected.

1.1 Related Documentation

VIP: Kit# 106913 - Intel $^{\mbox{\tiny (B)}}$ Ethernet Network Connections (20.1 OEM Gen) - LAN Software Production Candidate 20.1

1.2 Intel[®] ME FW Features

This firmware release includes the following applications:

- Platform Clocks Tune clock silicon to the parameters of a specific board, configure clocks at run time, and power management clocks. Benefit: Allows extensive customizability and soft control of "Third generation" clock solution and makes clocks available before CPU powers up.
- Silicon Workaround Capability Intel[®] ME FW will have limited capabilities to perform targeted workarounds for silicon issues. Benefit: Allows Intel[®] ME FW to address some issues that otherwise would require a new silicon stepping.

1.3 Prerequisites

Before this document is read and utilized, it is essential that the reader first review the Corporate FW Release Notes (included with this $Intel^{®}$ ME CorporateConsumer FW kit).



This document is constructed so that the reader can complete the bring up steps as given for the Intel Customer Reference Board (CRB). However, in the case that bring up is being performed on a different $Intel^{®}$ x based platform, this document will highlight any changes that must be imposed onto the bring up steps accordingly.

This document makes only the following limited assumptions regarding hardware:

- The platform is Intel[®] Skylake LP/H Chipset Family based
- The platform is equipped with one or more SPI Flash devices with a total capacity sufficient for storing all relevant firmware images.

1.4 Acronyms and Definitions

1.4.1 General

Acronym or Term	Definition
BIOS	Basic Input Output System
DIMM	Dual In-line Memory Module
DMI	Direct Media Interface
EC	Embedded Controller
FPF	Field Programmable Fuses
FW	Firmware
GbE	Gigabit Ethernet
HECI	Host Embedded Controller Interface (aka Intel [®] MEI)
Intel [®] ICCS	Intel [®] Integrated Clock Controller Service
Intel [®] ME	Intel [®] Management Engine (Intel [®] ME)
Intel [®] MEI	$Intel^{\textcircled{B}}$ Management Engine Interface (Intel^{\textcircled{B}} MEI) (renamed from HECI)
Intel [®] PTT	Intel [®] Platform Trusted Technology (Intel [®] PPT)
Intel [®] MSS	Intel® Management and Security Status Application
KVM	Keyboard, Video, Mouse
LAN	Local Area Network
MCP	Multi-Chip Package (Central Processing Unit / Platform Controller Hub)
NVM	Non-Volatile Memory
ООВ	Out-of-Band
OS	Operating System
PAVP	Protected Audio and Video Path
PCI	Peripheral Component Interconnect
PCIe*	Peripheral Component Interconnect Express
РНҮ	Physical Layer (Networking)
RTC	Real Time Clock
SBT	Intel [®] Small Business Technology
SMBus	System Management Bus
SPI Flash	Serial Peripheral Interface Flash
ТРМ	Trusted Platform Module
VSCC	Vendor Specific Configuration



1.4.2 Intel[®] Management Engine

Acronym or Term	Definition
3PDS	3rd Party Data Storage
Agent	Software that runs on a client PC with OS running
End User	The person who uses the computer (either Desktop or Mobile). In corporate, the user usually does not have administrator privileges. The end user may not be aware to the fact that the platform is managed by Intel [®] AMT.
Host or Host CPU	The processor that is running the operating system. This is different than the management processor running the Intel® Management Engine Firmware.
Host Service/Application	An application that is running on the host CPU
INF	An information file (.inf) used by Microsoft* operating systems that supports the Plug & Play feature. When installing a driver, this file provides the OS the necessary information about driver filenames, driver components, and supported hardware.
Intel [®] AMT Firmware	The Intel $^{\ensuremath{\mathbb{B}}}$ AMT Firmware running on the embedded processor
Intel [®] Management Engine Interface (Intel® MEI)	Interface between the Management Engine and the Host system
Intel [®] MEI driver	Intel^® ME host driver that runs on the host and interfaces between ISV Agents and the Intel^® ME HW.
IT User	Information Technology User. Typically very technical and uses a management console to ensure functionality of multiple PCs on a network.
LMS	Local Management Service: A SW application which runs on the host machine and provide a secured communication between the ISV agent and the Intel [®] Management Engine Firmware.
Intel [®] ME	$Intel^{\textcircled{B}}$ Management Engine: The embedded processor residing in the chipset MCP
Intel [®] MEBx	Intel [®] Management Engine BIOS Extensions
MECI	ME-VE Communication Interface
NVM	Non-Volatile Memory: A type of memory that will retain its contents even if power is removed. In the Intel [®] AMT current implementation, this is achieved using a FLASH memory device.
OOB Interface	Out Of Band interface: This is WSMAN interface over secure or non-secure TCP protocol.
OS not Functional	 The Host OS is considered non-functional in Sx power state and any one of the following cases when system is in S0 power state: OS is hung After PCI reset OS watch dog expires OS is not present
System States	Operating System power states such as S0. See detailed definitions in System States and Power Management section.
Un-configured state	The state of the Intel [®] Management Engine Firmware when it leaves the OEM factory. At this stage the Intel [®] Management Engine Firmware is not functional and must be configured.



1.4.3 System States and Power Management

Acronym or Term	Definition	
G3	A system state of Mechanical Off where all power is disconnected from the system. G3 power state does not necessarily indicate that RTC power is removed.	
СМО	Intel [®] Management Engine firmware power state where all hardware power planes are activated. The host power state is S0.	
СМЗ	Intel [®] Management Engine power state where the host is in Sx. The processor DRAM Controller is turned off and DRAM power stays in off/ self refresh mode. There is no UMA usage in CM3 state. Less than 1MB of SRAM used for code and data. Code is executed off of flash takes ~1mS.	
CM0-PG	Core Well Powered; Intel $^{\textcircled{B}}$ ME Well Powered; (Intel $^{\textcircled{B}}$ ME core not consuming power) DRAM available.	
CM3-PG	An Intel [®] ME Firmware power state where no power is applied to the Management Engine subsystem. (Intel [®] ME firmware is shut down).	
OS Hibernate	System state where the OS state is saved on the hard drive.	
SO	A system state where power is applied to all HW devices and the system is running normally.	
S1, S2, S3	A system state where the host CPU is halted but power remains available to the memory system (memory is in self-refresh mode).	
S4	A system state where the host CPU and memory are not active.	
S5	A system state where all power to the host system is off, however the power cord (and/or battery in mobile designs) is still connected.	
Shut Down	Equivalent to the S5 state.	
Snooze Mode	Intel [®] Management Engine activities are mostly suspended to save power. The Intel [®] Management Engine monitors HW activities and can restore its activities depending on the HW event.	
Standby	System state where the OS state is saved in memory and resumed from the memory when mouse/keyboard is clicked.	
Sx	All S states which are different than S0.	

1.5 Reference Documents

Document	Doc Number/ Location*
Skylake Intel [®] Management Engine (Intel® ME) and Embedded Controller Interaction Product Specification Revision 0.5	549024 / CDI
Intel [®] Management Engine BIOS Writers Guide	TBD / *
Intel [®] Management Engine (Intel® ME) 11 SKU Firmware Corporate Compliance Guide for Skylake PCH-H/LP Chipset Family - Skylake Platform Compliancy and Testing Guide - Revision 1.1	547409 / CDI

Note: * Unless specified otherwise, a document can be ordered by providing its reference number to your Intel Field Applications Engineer.

1.6 Format and Notation

The formats and notations used within this document model are those typically used by BIOS vendors. This section describes the formatting and the notations that will be followed in this document.



Table 1-1. Number Format Notation

Number Format	Notation	Example
Decimal (default)	d	14d. Note that any number without an explicit suffix can be assumed to be decimal.
Binary	b	1110b
Hex	h	0Eh
Hex	0x	0x0E

Table 1-2. Data Format Notation

Data Type	Notation	Size
Bit	b	Smallest unit, 0 or 1
Byte	В	8 bits
Word	W	16 bits or 2 bytes
Double-word	DW	32 bits or 4 bytes
Quad-word	QW	8 bytes or 4 words
Kilobyte	КВ	1024 bytes
Megabit	Mb	1,048,576 bits or 128 KB
Megabyte	MB	1,048,576 bytes or 1024 KB
Gigabit	Gb	1,073,741,824 bits
Gigabyte	GB	1024 MB



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1.7 Kit Contents

The Intel[®] ME Corporate FW kit can be downloaded from VIP (https://platformsw.intel.com/). The contents of this kit are detailed below (Note that only key files are listed).

Table 1-3. Kit Contents (Sheet 1 of 4)

Content Description		
Root directory		
This document		
How to program SPI device parameters and descriptor region details. Also contains a complete SPI Flash softstrap reference.		
How to program SPI device parameters and descriptor region details. Also contains a complete SPI Flash softstrap reference.		
BIOS image only for Intel CRB.		
BIOS image only for Intel CRB.		
Intel [®] LAN PHY LPT-H firmware image.		
Intel [®] LAN PHY LPT-LP firmware image.		
Intel [®] ME firmware image (Non Production FW Rom Bypass) - supports unfused Skyla PCH-LP Platform I/O MCP steppings: • Unfused (Super SKU) Note: For PAVP Testing, you must match Production FW with Production Part and Non Production FW with Non Production Parts.		
Intel [®] ME firmware image (Non Productior FW) - supports unfused Skylake PCH-LP Platform I/O MCP steppings: • Unfused (Super SKU) Note: For PAVP Testing , you must match Production FW with Production Part and Non		
Production FW with Non Production Parts.		

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Table 1-3. Kit Contents (Sheet 2 of 4)

File or [Dire	ctory]	Content Description
Intel®_	ME SW Installation Guide.pdf	Intel [®] ME Software installation Guide.
Intel®_	MSS User Guide.pdf	
[ME_SW	/_MSI]	
[Pre	eProduction]	
	IntelMEFWVer.dll	
	MUP	XML file
	SetupME	
	WixLicenseNote.txt	
[MEI-Or	nly Installer MSI]	
Inte	elMEFWVer.dll	
MEI	Setup	
MUR	2	XML file
[Tools]		
[100	C_Tools]	
	Intel® ME Firmware Integrated Clock Control (ICC) Tools User Guide.pdf	ICC Tools User Guide
	[CCT]	
	cct	Exe file
	cct	Ini file
	cctDII.dll	
	cctWin	Exe file
	[EFI]	
	cct.efi	CCT for EFI
[Sy:	stem Tools]	
	Open Watcom Public License.pdf	Sybase Open Watcom Public License version 1.0 document.
	System Tools User Guide.pdf	System Tools User Guide
	[Flash Image Tool]	
	fit.exe	Intel® Flash Image Tool (Intel® FIT)
	newfiletmpl.xml	FITC Configuration XML file
	vsccommn.bin	Binary containing the supported SPI parts
	VSCCommn_bin Content.pdf	Documentation listing the SPI parts supported by vscccommn.bin
	[Flash Programming Tool]	
	[DOS]	
	fparts.txt	List of supported SPI Flash devices with specific Flash parameters
	fpt.exe	Intel® FPT for DOS
	[EF164]	
	fparts.txt	List of supported SPI Flash devices with specific Flash parameters
	fot efi	Intel® EPT for EEL
	ipt.en	



Table 1-3. Kit Contents (Sheet 3 of 4)

File or [Directory]	Content Description
[Windows]	
fparts.txt	List of supported SPI Flash devices with specific Flash parameters
fptw.exe	Intel® FPT for Windows*
l drvdll.dll	
Pmxdll.dll	
[Windows64]	
fparts.txt	List of supported SPI Flash devices with specific Flash parameters
fptw64.exe	Intel® FPT for Windows* (64-bit) OS
Idrvdli32e.dli	
Pmxdll32e.dll	
[FWUpdate]	
[EFI64]	
FWUpdLcl.efi	FW Update Tool (EFI version)
[DOS]	
FWUpdLcl.exe	FW Update Tool (DOS version)
[Win]	
FWUpdLcl.exe	FW Update Tool (Windows* version 32bit)
[Win64]	
FWUpdLcl64.exe	FW Update Tool (Windows* version 64bit)
[Manifest Extension Utility]	
[Win]	
meu.exe	Intel [®] Manifest Extension Utility (MEU) executable file that allows input of FW binary and outputs and independent updatable partition that is compressed and signed.
[MEInfo]	
[DOS]	
MEInfo.exe	Intel [®] ME Information Tool (DOS version)
[EFI64]	
MEInfo.efi	Intel [®] ME Information Tool (EFI version)
[Windows]	
MEI nfoWin.exe	Intel [®] ME Information Tool (Windows* version 32bit)
Idrvdll.dll	
Pmxdll.dll	
I SHLib.dll	
[Windows64]	
MEInfoWin64.exe	Intel [®] ME Information Tool (Windows* version 64bit)
Idrvdll32e.dll	
ISHLib.dll	



File or [Directory]		Content Description
	Pmxdll32e.dll	
[MEManu	if]	
[DC	DS]	
	MEManuf.exe	Intel [®] ME Manufacturing Tool (DOS version)
	vsccommn.bin	Binary containing the supported SPI parts
	VSCCommn_bin Content.pdf	Documentation listing the SPI parts supported by vscccommn.bin
[EF	164]	
	VSCCommn_bin Content.pdf	Documentation listing the SPI parts supported by vscccommn.bin
	MEManuf.efi	Intel [®] ME Manufacturing Tool (EFI version)
	vsccommn.bin	Binary containing the supported SPI parts
[Wi	indows]	
	Idrvdll.dll	
	MEManufWin.exe	Intel [®] ME Manufacturing Tool (Windows* version 32bit)
	Pmxdll.dll	
	ISHLib.dll	
	vsccommn.bin	Binary containing the supported SPI parts
	VSCCommn_bin Content.pdf	Documentation listing the SPI parts supported by vscccommn.bin
[Wi	indows64]	
	Idrvdll32e.dll	
	ISHLib.dll	
	MEManufWin64.exe	Intel [®] ME Manufacturing Tool (Windows* version 64bit)
	Pmxdll32e.dll	
	vsccommn.bin	Binary containing the supported SPI parts
	VSCCommn_bin Content.pdf	Documentation listing the SPI parts supported by vscccommn.bin
(empty)		

Table 1-3.Kit Contents (Sheet 4 of 4)



1.8 External Hardware Requirements for Bring Up

Acquire the following hardware tools before moving on to the next step.

Windows* OS System	Flash Burner	DOS Bootable USB Key
Equipment: • Laptop or desktop that supports win32 applications Purpose: • Will run firmware image assembly and build process software.	 Equipment: (Optional) For platforms that don't boot, a Flash Chip Programmer will be required For platforms that can boot to DOS or Windows*, a Intel® FPT is provided in this kit Purpose: Will burn firmware images onto the target system Flash device(s). 	 Equipment: A DOS Bootable USB Key (Size > 512 MB) Purpose: Acting as a bootable device and will be used to run Intel® FPT (Fpt.exe) directly on the system that is undergoing Bring Up process. Or will be used to transfer a firmware image onto a Flash burner.

§§



2 Image Creation: Intel[®] Flash Image Tool

Intel[®] Flash Image Tool (Intel[®] FIT) can be used to generate either a full SPI Flash binary image with Descriptor, GbE, BIOS, and Intel[®] ME Regions. Additionally, it can be used to create a simple image containing only the Intel[®] ME Region only for use with custom SPI Flash binary image assembly solutions. Use the steps shown in following sections.

After this image has been created, it will need to be burned onto the target platform's SPI Flash device(s). Section 3, "Programming SPI Flash Devices and Checking Firmware Status" later in this document provides steps to do this.

Note: The Flash Image Tool may be updated throughout the release cycles. As a general rule, please ensure you use the tools, images and other content from the same kit and refrain from using different version tools.

2.1 Start Intel[®]FIT

- Invoke Intel[®] Flash Image Tool. Using Explorer*, navigate to [root]\Tools\System Tools\Flash Image Tool. Verify that the directory contents are correct (see Section 1.7). Double-click FIT.exe.
- 2. **NOTE:** In the tables below, where default settings are listed for SKL LP/H, if the value is the same one value will be listed. If there is a different default value when the program loads with either platform, both values will be listed to show the difference.

2.2 Step-by-Step Guide to Build SPI Flash Image with Intel[®] FIT Interface



#	Label	Label Contents				
	🚆 Intel ® Flash Image Tool			- • ×		
	File Build Help					
		Intel (R) LP Series	Chipset 🔹 Premium U 🔹			
	Flash Layout	Intel(R) ME Binary File				
	Flash Settings					
	Intel (R) ME Kernel	DDD Dealon				
	Intel (R) AMT					
	Platform Protection	0				
	Integrated Clock Controller	00				
	Networking & Connectivity	PDR Region Enable	Disabled			
	FlexI/O	BIOS Region				
	Internal PCH Buses	bios Region				
	GPIO	Parameter	Value			
	Power	Length	0	•		
	Integrated Sensor Hub	BIOS Binary File				
	Debug	BIOS Region Enable	Disabled	·		
	CPU Straps			E.		
	Initializing Using vsccommn.bin with tim Ready to build.	nestamp 22:48:59 02/21/2014	GMT	•		
1	Button Interface	This button labeled 'N values	lew' on rollover allows open	ing of a new session with default		
2	Button Interface	This button labeled 'C	Open' on rollover allows oper	ning of an xml or bin file		
3	Button Interface	This button labeled 'S	Save' on rollover allows savii	ng of xml file		
4	Button Interface	This button labeled 'C	Clear Console' clears the con	sole area (see page 23)		
6	Button Interface	This button labeled 'E (Table 2-2)	Build Settings' brings up the	build settings popup Window see		
6	Button Interface	This button labeled 'E	Build Image' on rollover allov	ws build of the image		

Table 2-1. Intel[®] FIT - Initial Screen Layout (Sheet 1 of 7)



#	Label			Contents		
	File Build Help	Intel (R) LP Series Cl	7 - Pi	remium U 🔼 -	- • X	
	Flash Layout Flash Settings Intel (R) ME Kernel	Intel(R) ME Binary File		Ţ	·	
	Intel (R) AMT Intel (R) Platform Protec Integrated Cloc Networking & Connectivity	LP Series Chipset H Series Chipset PDR Region Enable	0 Disabled	Premium U Base U Premium Y LP No Emulation		
	Flex I/O Internal PCH Buses GPIO	 BIOS Region 		Value		
	Power Integrated Sensor Hub Debug	Length BIOS Binary File BIOS Region Enable	0 Disabled	- Criev	- -	
	CPU Straps 08/27/2014 14:40:20 Initializing Using vsccommn.bin with tin Ready to build.	nestamp 22:48:59 02/21/2014 G	мт			
7	Drop Down Selector	This drop down allows	selection of	f platform		
8	Drop Down Selector	This drop down allows	selection of	^F SKU within platfo	rm selected	

 Table 2-1.
 Intel[®] FIT - Initial Screen Layout (Sheet 2 of 7)



Label Cont				ents		
	🕎 Intel ® Flash Image Tool				<u> </u>	I X
	File Build Help					
		6 🛛 🛛	intel (R) LP Series	Chipset 👻 Premium U	×	
	Flash Layout	Intel(R) M	E Binary File			-
	Flash Settings	inconfred in	e omary rine			- 11
	Intel (R) ME Kernel	PDR	Region			
	Intel (R) AMT		Parameter	Value	Ĩ	
	Platform Protection	Length		0	-	
	Integrated Clock Controller	PDR Bina	Flash Lav	out 9		
	Networking & Connectivity	PDR Reg	11001120,		2	
	Flex I/O		Flash Sett	inas 10	1	
	Internal PCH Buses	➡ BIO			-	
	GPIO		Intel (R) M	E Kernel 11		
	Power	Length				
	Integrated Sensor Hub	BIOS Bin	ary File			
	Debug	BIOS Reg	ion Enable	Disabled		1
	CPU Straps	4				• •
	08/27/2014 14:40:20 Initializing Using vsccommn.bin with Ready to build.	limestamp 22	2:48:59 02/21/2014	GMT		*

Table 2-1. Intel[®] FIT - Initial Screen Layout (Sheet 3 of 7)



#	Label	Contents
		Flash Layout which contains (see Table 2-3):
9	Flash Layout Tab	Regions Descriptor Region GBE Region Intel® ME Region PDR Region EC Region BIOS Region
		Flash Settings which contains (see Table 2-4):
		Flash Components
		Host CPU/ BIOS Master Access
		Intel® ME Master Access
	Flash Settings Tab	GBE Master Access
		EC Master Access
		Flash Configuration
		VSCC Table - VSCC Entry
		SPI based RPMC Configuration
		BIOS Configuration
		Intel® ME Kernel which contains (see Table 2-5):
		Processor
		Intel® ME Firmware Update
	Intel® ME Kernel Tab	Intel® Services Configuration
		Image Identification
		MCTP Configuration
		Firmware Diagnostics
		Post Manufacturing Lock
		Reserved

Table 2-1.	Intel®	FIT -	Initial	Screen	Layout	(Sheet 4	of 7)



#	Label	Contents
	Intel ® Flash Image Tool	_ _ X
	File Build Help	
		Intel (R) LP Series Chipset Premium U
	Flash Layout	Intel(R) ME Binary File
	Flash Settings	- DDD Declar
	Intel (R) ME Kernel	• PDR Region
	Intel (R) AMT	F Intel (R) AMT
	Platform Protection	Length -
	Integrated Clock Controller	PDR Binary Platform Protection 13
	Networking & Connectivity	PDR Region
	Flex I/O	- noc Integrated Clock Contr. 14
	Internal PCH Buses	
	GPIO	F Networking & Connect 15
	Power	Length
	Integrated Sensor Hub	BIOS Binary File -
	Debug	BIOS Region Enable Disabled -
	CPU Straps	• • • • •
	Using vsccmmn.bin with tin Ready to build.	nestamp 22:48:59 02/21/2014 GMT
12	Intel® AMT Tab	Intel® AMT which contains (see Table 2-6): Intel® AMT Configuration KVM Configuration Provisioning Configuration OEM Customizable Certificates (1, 2, 3) OEM Default Certificates (1, 2, 3, 4, 5) Redirection Configuration TLS Configuration
13	Platform Protection Tab	 Platform Protection which contains (see Table 2-7): Content Protection Graphics uController Hash Key Configuration for Bootguard / ISH Boot Guard Configuration Intel® PTT Configuration TPM Over SPI Bus Configuration
14	Integrated Clock Controller Tab	 Integrated Clock Controller which contains (see Table 2-8): Integrated Clock Controller Policies Profiles
15	Networking & Connectivity Tab	 Networking & Connectivity which contains (see Table 2-9): Wired LAN Configuration Wireless LAN Configuration Intel® NFC Configuration

 Table 2-1.
 Intel[®] FIT - Initial Screen Layout (Sheet 5 of 7)



#	Label	Contents
#	Label	Contents
	Power Integrated Sensor Hub	Length - BIOS Binary File -
	Debug CPU Straps 08/27/2014 14:40:20	BIOS Region Enable Disabled -
	Initializing Using vsccommn.bin with tin Ready to build.	restamp 22:48:59 02/21/2014 GMT
16	Flex I/O Tab	Flex I/O which contains (see Table 2-10): Intel® RST for PCIe Configuration PCIe Lane Reversal Configuration PCIe Port Configuration SATA / PCIe Combo Port Configuration SATA / PCIe Combo Port Select Polarity USB3 Port Configuration XHCI Port Configuration
17	Internal PCH Buses Tab	Internal PCH Buses which contains (see Table 2-11): OPI Configuration DMI Configuration eSPI Configuration PCH Timer Configuration SMBus / SMLink Configuration
18	GPIO Tab	 GPIO which contains (see Table 2-12): LAN / GPIO Select WLAN / GPIO Select Platform Power / GPIO ME Feature Pins
19	Power Tab	Power which contains (see Table 2-13): Platform Power Intel® ME Power Configuration Deep Sx

 Table 2-1.
 Intel[®] FIT - Initial Screen Layout (Sheet 6 of 7)



#	Label	Contents
	Intel ® Flash Image Tool File Build Help	
		Volume Intel (R) LP Series Chipset V Premium U V
	Flash Layout	Intel(R) ME Binary File -
	Flash Settings	▼ PDR Region
	Intel (R) ME Kernei	
	Platform Protection	Parameter Value
	Integrated Clock Controller	PDR Binary Integrated Sensor Hul 20
	Networking & Connectivity	PDR Region
	Flex I/O	Debug 21
	Internal PCH Buses	CPU Straps 22
	GPIO	
	Power	Length 0 -
	Debug	BIOS Binary File -
	CPU Straps	
	08/27/2014 14:40:20 Initializing Using vsccommn.bin with tin Ready to build.	nestamp 22:48:59 02/21/2014 GMT
20	Integrated Sensor Hub Tab	Integrated Sensor Hub which contains (see Table 2-14): Integrated Sensor Hub ISH Image ISH Data
21	Debug Tab	 Debug which contains (see Table 2-15): Intel® ME Firmware Debugging Overrides Direct Connection Interface Configuration Intel® Trace Hub Technology
22	CPU Straps Tab	CPU Straps which contain a detailed list of parameters (see Table 2-16)
23	Console Window Area	Displays opening messages, log file entries, and build activity messages

Table 2-1. Intel[®] FIT - Initial Screen Layout (Sheet 7 of 7)



		0910	Jerringe .	-			
	Build Settings						
 Image Build Setting 	 Image Build Settings 						
Parameter	Valu	e	Help Text				
Output Path	outimage.bin		0	_			
Generate Intermediate Files	Yes		2				
Enable Boot Guard warning me	Yes		3				
Enable Intel (R) Platform Trust	Yes		4				
CPU Stepping	Stepping B		5				
Region Order	32451		6				
 Environment Variab 	les						
Parameter	Valu	e	Help Text	=			
\$WorkingDir	*.)		Path for environment variable \$WorkingDir				
\$SourceDir			Path for environment variable \$SourceDir				
\$DestDir	•		Path for environment variable \$DestDir				
dian Mus			- Auth for aminument-rariable dilauthart				
\$UserVar2			Path for environment variable \$UserVar2				
\$UserVar3			Path for environment variable \$UserVar3				
	1	T					
Parameter	CRB		Values				
Output Path		Double specify outimag	click to the right of outimage.bin and click to get bro path and name of file to create for the build - defau ge.bin in the same folder as Intel® FIT tool	owse bu ılt is			
Generate Intermediate Files	Yes	Yes/No	- Yes is default				
Enable Boot Guard warning message at build time	Yes	Yes/No	- Yes is default				
		Voc/No	- Yes is default				
Enable Intel(R) Platform Trust Technology warning message at build time	Yes	165/100					

Table 2-2. Intel[®] FIT - Build Settings (Sheet 1 of 2)



Table 2-2. Intel[®] FIT - Build Settings (Sheet 2 of 2)

Click on	Build Button in th	e top menu bar> Build S	Settings window pop up is displaye	d:		
#	Parameter	CRB	Value	es		
6	Region Order	r				
		9	WorkingDir and \$DestDir can be left a	t the default '.'		
0			Click on \$SourceDir Value field and type Components are located for the Manage	e in path where eability Engine	the Ima kit	је
Table	2-3. Intel [®] F	TT - Flash Layout	(Sheet 1 of 5)			
Click o	n Flash Layout in tl	he left tabs menu> Dese	criptor Region is expanded by defa	ult:		
▼ Des	criptor Region	1				
	Parameter	Value	Help Text		_	
Length		0	-			
OEM Se	OEM Section Binary -					
#	# Parameter		ter	Platform	Se	ttings
1	Descriptor Region Values: Leave this length.	n - Length is at zero. Allows Intel® F	FIT to auto-size the descriptor region	-size the descriptor region SKL-Y 0 SKL-U 0 SKL-H 0 SKL-S 0		
	OEM Section Bina This loads the OEM generated by the I	ary I Section binary that will be ntel® FIT tool.	e merged into the output image			
Click of	n Flash Layout in ti	he left tabs menu> Gbe	Region is expanded by default:			
	Daramator	Value	Holp Toxt			
L ength	Falameter	0	- Tielp Text			
GbE Bin	ary File	-	-			
GbE Reg	jion Enable	Enabled	-			
Image Id		0	-			
Major Ve	rsion	0	-			
Minor Ve	rsion	0	-			



Table 2-3. Intel[®] FIT - Flash Layout (Sheet 2 of 5)

#	Parameter		Platform	Settings	
2	GbE Region - Length Note: This value will be automatically populated I	ge build.	SKL-Y SKL-U SKL-H SKL-S	0 0 0 0	
	GbE Binary File Navigate to your Source Directory (as specified GbE subdirectory. Choose the appropriate Intel Gk not using Intel LAN then load the GbE image along with changing additional settings belo integrated LAN binary that will be merged into the Intel® FIT tool. Note: If loading gbeimage.bin file, check that the before building image.	to the mage. If egion I by the tool	SKL-Y SKL-U SKL-H SKL-S	gbeimage.bin gbeimage.bin gbeimage.bin gbeimage.bin	
	GbE Region Enable Values: Enabled/Disabled - This option allows the user to enable or disable the Gigabit Ethernet Region. NOTE: If choosing a configuration that does not include the GbE LAN the following settings need to be adjusted:				Enabled Enabled Enabled Enabled
These ac GPIO S	Name LAN PHY Power Control GPD11 Signal Configuration Gbe MAC SMBus Address Enable PHY Connection Intel® PHY Over PCIe Enable Intel® Integrated wired LAN Enable Idditional settings are under the Networking & Corelect ensure the value is set correctly for board type	Location Offset 0x164 [7:6] LP Offset 0x1A0 [7:6] H Offset 0x1A0 [7:6] H Offset 0x147 [0] LP Offset 0x147 [0] LP Offset 0x192 [2:0] LP Offset 0x10E [2:0] H Offset 0x10E [2:0] H Offset 0x10E [6] LP Offset 0x1BE [6] H Offset 0x1BC [6] LP Offset 0x20C [6] H Interctivity tab > Wired I Dec.	Value 00b 0b 0b 0b .AN Confi	iguration. In th	ne GPIO > LAN /
	Image Id - This displays Image ID of the current binary. Major Version - This displays Major revision num	ted LAN ed			
	Minor Version - This displays Minor revision nun Intel® Integrated LAN binary.	nber of the currently load	ed		



Intel(R) ME Region

Table 2-3. Intel[®] FIT - Flash Layout (Sheet 3 of 5)

3

Click on Flash Layout in the left tabs menu> Intel® ME Region is expanded by default:

Parameter	Value	Help Text
Length	0	-
Intel(R) ME Binary File		This loads the Intel (R) ME binary that will be merged into t
Major Version	0	This displays Major revision number of the currently loaded
Minor Version	0	This displays Minor revision number of the currently loaded
Hotfix Version	0	This displays Hot-Fix revision number of the currently loade
Build Version	0	This displays Build version number of the currently loaded I
Chipset Initialization Version		This displays the current Chipset Initialization version contain
Chipset Initialization Binary		This loads the Chipset Initialization binary that will be merge
ChipsetInit Override Version		This displays the version of the Chipset Initialization Binary
Intel (R) Trace Hub Binary		This loads the Intel (R) Trace Hub binary that will be merge

#	Parameter	Platform	Settings
	Intel® ME Region - Length	SKL-Y	0
		SKL-U	0
3		SKL-H	0
		SKL-S	0
	Intel® ME Binary File	SKL-Y	meimage.bin
	Navigate to your Source Directory (as specified in Table 2-2) and switch to the ME	SKL-U	meimage.bin
	subdirectory. Choose the appropriate Intel ME Firmware binary image. This loads	SKL-H	meimage.bin
	by the Intel® FIT tool.	SKL-S	meimage.bin
	Note: You may choose to build the Intel® ME Region only. To do so, the Number of Flash Components in Flash Settings> Flash Components must be set to 0.		
	Note: If loading meimage.bin file, check that the ME region is enabled in tool before building image.		
	Major Version - This displays Major revision number of the currently loaded Intel® ME binary.		
	Minor Version - This displays Minor revision number of the currently loaded Intel® ME binary.		
	Hotfix Version - This displays Hot-Fix revision number of the currently loaded Intel® ME binary.		
	${\rm Build}\ {\rm Version}\ {\rm -}\ {\rm This}\ {\rm displays}\ {\rm Build}\ {\rm version}\ {\rm number}\ {\rm of}\ {\rm the}\ {\rm currently}\ {\rm loaded}\ {\rm Intel}\ {\rm \ensuremath{\mathbb{B}}\ }$ ME binary.		
	Chipset Initialization Binary - This loads the Chipset Initialization binary that will be merged into the output image generated by the Intel® FIT. If specified, this will override the version contained in the Intel® ME binary.		
	Chipset Initialization Version - This displays the current Chipset Initialization version contained in the currently loaded Intel® ME binary.		
	ChipsetInit Override Version - This displays the version of the Chipset Initialization Binary override if specified.		
	Intel® Trace Hub Binary - This loads the Intel® Trace Hub binary that will be merged into the output image generated by the Intel® FIT tool.		



Table 2-3. Intel[®] FIT - Flash Layout (Sheet 4 of 5)

Click or	Click on Flash Layout in the left tabs menu> PDR Region is expanded by default:						
▼ PDF	R Region	4					
	Parameter Value Help Text						
Length		0	-				
PDR Bina	ıry File		-				
PDR Reg	PDR Region Enable Disabled -						
#	Parameter			Platform	Settings		
	PDR Region - Length			SKL-Y	0		
	Region is disabled I	oy default. Displays Regio	on size information when Binary input	SKL-U	0		
4 file is specified.			SKL-H	0			
			SKL-S	0			
	PDR Binary File			SKL-Y	-		
	Navigate to path to	load pdrimage.bin file if	required and available. This loads the	SKL-U	-		
	Platform Data regio	on binary that will be mer	ged into the output image generated by	SKL-H	-		
	the Intel® FIT tool	•		SKL-S	-		
	PDR Region Enab	le		SKL-Y	Disable	ed	
	Values: Enabled/Disabled - This option allows the user to enable or disable the			SKL-U	Disable	∋d	
	Platform Data Region.			SKL-H	Disable	∋d	
	Note: If loading PDR.bin file, check that the PDR region is enabled in tool before building image.					эd	
Click or	n Flash Layout in th	ne left tabs menu> Ec	Region is expanded by default:				

EcRegion



Parameter	Value	Help Text
Length	0	-
EC Binary File		This loads the Embedded Controller binary used for eSPI that
EC Region Enable	Disabled	This option allows the user to enable or disable the Embedded

#	Parameter	Platform	Settings
	EC Region - Length	SKL-Y	0
		SKL-U	0
5		SKL-H	0
		SKL-S	0
	EC Binary File	SKL-Y	
	Navigate to path to load EC bin file. This loads the Embedded Controller binary used	SKL-U	
	for eSPI that will be merged into the output image generated by the Intel® FIT	SKL-H	
	tool.	SKL-S	
	EC Region Enable	SKL-Y	Disabled
	Values: Enabled/Disabled	SKL-U	Disabled
	This option allows the user to enable or disable the Embedded Controller data	SKL-H	Disabled
	region.	SKL-S	Disabled



Table 2-3. Intel[®] FIT - Flash Layout (Sheet 5 of 5)

6

Click on Flash Layout in the left tabs menu> BIOS Region is expanded by default:

BIOS Region

1	Parameter	Value	Help Text			
Length		0				
BIOS Binary	/ File		This loads the BIOS binary that will be merged into the output image generated by the Int			
BIOS Region Enable Enabled This option allows the user to enable or disable the Bios Region.						
# Parameter Platform Setting					Settings	

#	Parameter	Platform	Settings
	BIOS Region - Length	SKL-Y	0
		SKL-U	0
6		SKL-H	0
		SKL-S	0
	BIOS Binary File	SKL-Y	
	Navigate to path to load bios.rom file. This loads the BIOS binary that will be	SKL-U	
merged into the output image generated by the Intel® FIT tool.		SKL-H	
		SKL-S	
	BIOS Region Enable	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	This option allows the user to enable or disable the BIOS region.	SKL-H	Enabled
	Note: After loading bios.rom file, check that the BIOS region is enabled in tool before building image.	SKL-S	Enabled



▼ Fla	sh Components	; 1				
	Parameter	Value		Help Text		
Number	of Flash Components	5 2	This setting configures the tot	total number of flash components fo		
Flash co	omponent 1 Size	8MB	This setting determines the si	size of Flash component 1 for the pla		
Flash co	component 2 Size 8MB This setting determines the size of			ze of Flash com	ponent 2 for the p	
SPI Volt	age Select	3.3 Volts	This strap sets the internal co	ntrol signal on t	he pad for either 1	
#		Paramet	ter	Platform	Settings	
1	Flash Componen	ts				
	Number of Comp Values: 0, 1, 2 - the platform. Note build an output im	SKL-Y SKL-U SKL-H SKL-S	1 1 1 1			
	Flash component Values: 512KB, 1 determines the siz	SKL-Y SKL-U SKL-H SKL-S	8MB 16MB 16MB 16MB			
	Flash component Values: 512KB, 1 determines the siz is only applicable v	t 2 Size I MB, 2MB, 4MB, 8MB, 16N e of Flash component 2 for t vhen the Number of Flash C	MB, 32MB, 64MB - This setting the platform image. Note: This setting Components option is set to '2'.	SKL-Y SKL-U SKL-H SKL-S	8MB 8MB 8MB 8MB	
	SPI Voltage Sele Values: 1.8 Volts for either 1.8 or 3. details.	ct ;, 3.3 Volts - This strap set: 3 volts. See Skylake H / LP	s the internal control signal on the pad SPI Programming Guide for further	SKL-Y SKL-U SKL-H SKL-S	3.3 Volts 3.3 Volts 3.3 Volts 3.3 Volts 3.3 Volts	
Click or	Flash Settings in	the left tabs menu> Hos	t CPU/BIOS Master Access is expan	ded by defaul	t:	
▼ Ho	st CPU / BIOS Mas	ter Access 2				
	Parameter	Value	Help Text			
Host CPI	U / BIOS Write Access	0xFFF	- ·			
Host CPI	U / BIOS Read Access	0xFFF				
#	1	Paramet	ter	Platform	Settings	
2	Host CPU / BIOS	Master Access				

Table 2-4. Intel[®] FIT - Flash Settings (Sheet 1 of 7)



Table 2-4. Intel[®] FIT - Flash Settings (Sheet 2 of 7)

#	Parameter			Platform	Settings	
#	Parameter Host CPU / BIOS Write Access Values: 0xFFF, 0x00A, 0x01A - This setting determines write access control for the BIOS region. OxFFF = Debug/Manufacturing 0x00A = Production Ox01A = Production with access to PDR (should ONLY be used if PDR region is implemented). For further details on Region Access Control see Skylake H / LP SPI Programming guide further details. Host CPU / BIOS Read Access Values: 0xFFF, 0x00B, 0x01B - This setting determines read access control for the BIOS region. 0xFFF = Debug/Manufacturing 0x00B = Production with access to PDR (should ONLY be used if PDR region is implemented). Ox IB = Production with access to PDR (should ONLY be used if PDR region is implemented).				Settings 0xFFF 0xFFF 0xFFF 0xFFF 0xFFF 0xFFF 0xFFF 0xFFF 0xFFF	
	guide.	on Region Access Control see	e Skylake H / LP SPI Programming			
Click on	Flash Settings in	the left tabs menu> Intel	® ME Master Access is expanded by	y default:		
Parameter Value Help Text Intel(R) ME Write Access 0xFFF -						
Intel(R) M	E Read Access	UXFFF	-	1		
#		Paramete	r	Platform	Settings	
3	Intel® ME Master Access Intel® ME Write Access Values: 0xFFF, 0x00C - This setting determines write access control for the ME region. 0xFFF = Debug/Manufacturing 0x00C = Production			SKL-Y SKL-U SKL-H SKL-S	OxFFF OxFFF OxFFF OxFFF	
	For further details on Region Access Control see Skylake H / LP SPI Programming guide further details.					
	Intel® ME Read Access Values: 0xFFF, 0x00D - This setting determines read access control for the ME region. 0xFFF = Debug/Manufacturing 0x00D = Production For further details on Region Access Control see Skylake H / LP SPI Programming guide further details.			SKL-Y SKL-U SKL-H SKL-S	OxFFF OxFFF OxFFF OxFFF	
Click on Flash Settings in the left tabs menu> GbE Master Access is expanded by default:						
▼ GbE Master Access 4						
Parameter Value Help Text						
GbE Writ		A. FFF				
	e Access	UXFFF	-			



Table 2-4.	I ntel [®]	FIT -	Flash	Settings	(Sheet 3	of 7)
------------	---------------------	-------	-------	-----------------	----------	-------

#	Parameter			Platform	Settings
	GbE Master Access				
4					
	GbE Write Access			SKL-Y	OxFFF
	Values: 0xFFF, 0x008 Ethernet Region.	- This setting determines write	e access control for the Gigabit	SKL-U SKL-H	OxFFF OxFFF
	0xFFF = Debug/Manufa 0x008 = Production	cturing		SKL-S	OxFFF
	For further details on Re guide further details.	gion Access Control see Skyla	ke H / LP SPI Programming		
	GbE Read Access	T I III III I		SKL-Y	OxFFF
	Ethernet Region.	- This setting determines read	d access control for the Gigabit	SKL-U SKL-H	0xFFF 0xFFF
	0xFFF = Debug/Manufa	cturing		SKL-S	OxFFF
	0x008 = Production				
	For further details on Re guide further details.	gion Access Control see Skyla	ke H / LP SPI Programming		
Click or	Flash Settings in the le	eft tabs menu> EC Master /	Access is expanded by defau	It:	
– E	C Master Access	6			
		-			
	Darameter	Value		Hole Text	
	Parameter	vdiue		Help Text	
Embedo	Embedded Controller Write Acc 0xFFF This setting determines we		rite access contr	ol for the Embedde	
Embedo	ded Controller Read Acc	0xFFF	This setting determines re	ad access contro	ol for the Embeddeo
۱ #	Parameter			Platform	Settings
	EC Master Access				J
5					
#	Parameter			Platform	Settings
	EC Write Access			SKL-Y	OxFFF
	Values: 0xFFF, 0x020 - This setting determines write access control for the				OxFFF
	OxFFF = Debug/Manufa	SKL-H	UXFFF OVEEE		
	0x020 = Production				UXFFF
	For further details on Region Access Control see Skylake H / LP SPI Programming guide further details.				
	EC Read Access				OxFFF
	Values: 0xFFF, 0x008 - This setting determines read access control for the				OxFFF
	Embedded Controller Region.				UXFFF
	0xFFF = Debug/manufacturing 0x020 = Production				UXFFF
	For further details on Region Access Control see Skylake H / LP SPI Programming guide further details.				



Table 2-4. Intel[®] FIT - Flash Settings (Sheet 4 of 7)

6

Click on Flash Settings in the left tabs menu> Flash Configuration is expanded by default:

Flash Configuration

Parameter	Value	Help Text
Dual I/O Read Enabled	No	This setting allows customers to enable support for Dual I/O Read capabilitie
Dual Output Read Enabled	No	This setting allows customers to enable support for Dual Output Read capabi
Fast Read clock frequency	17MHz	This setting allows customers to configure the flash component clock freque
Fast Read supported	No	This setting allows customers to enable support for Fast Read capabilities fo
Invalid Instruction 0	0x0	This setting allows customers to configure invalid instruction to protect again
Invalid Instruction 1	0x0	This setting allows customers to configure invalid instruction to protect again
Invalid Instruction 2	0x0	This setting allows customers to configure invalid instruction to protect again
Invalid Instruction 3	0x0	This setting allows customers to configure invalid instruction to protect again
Invalid Instruction 4	0x0	This setting allows customers to configure invalid instruction to protect again
Invalid Instruction 5	0x0	This setting allows customers to configure invalid instruction to protect again
Invalid Instruction 6	0x0	This setting allows customers to configure invalid instruction to protect again
Invalid Instruction 7	0x0	This setting allows customers to configure invalid instruction to protect again
Quad I/O Read Enabled	No	This setting allows customers to enable support for Quad I/O Read capabiliti
Quad Output Read Enabled	No	This setting allows customers to enable support for Quad Output Read capa
Read ID and Read Status clock	17MHz	This setting allows customers to configure the flash component clock freque
Write and Erase clock frequency	17MHz	This setting allows customers to configure the flash component clock freque

#	Parameter		Settings
	Flash Configuration		
6			
	Dual I/O Read Enabled	SKL-Y	No
	Values: Yes/No - This setting allows the customer to enable support for Dual I/O	SKL-U	No
	Read capabilities for flash components. See Skylake H / LP SPI Programming guide	SKL-H	No
	for further details.	SKL-S	No
	Dual Output Read Enabled	SKL-Y	No
	Values: Yes/No - This setting allows the customer to enable support for Dual	SKL-U	No
	Output Read capabilities for flash components. See Skylake H / LP SPI Programming	SKL-H	No
	guide for further details.		Yes



Table 2-4. Intel[®] FIT - Flash Settings (Sheet 5 of 7)

#	Parameter	Platform	Settings
	Fast Read Clock Frequency	SKL-Y	48MHz
	Values: 17MHz, 30MHz, 48MHz - This setting allows the customer to configure the	SKL-U	48MHz
	flash component clock frequency setting for Fast Read. See Skylake H / LP SPI	SKL-H	48MHz
	Programming guide for further details.	SKL-S	48MHz
	Fast Read Supported	SKL-Y	Yes
	Values: Yes/No - This setting allows the customer to enable support for Fast Read	SKL-U	Yes
	capabilities for flash components. See Skylake H / LP SPI Programming guide for	SKI-H	Yes
	further details.	SKL-S	Yes
	Note: If fast read supported is set to "No" any changes made to Dual I/O, Quad I/O, or Quad Output will not be affected if set to yes. Fast read supported should also be set to enable frequencies greater than 20MHz.		
	Invalid Instruction 0 - This setting allows the customer to configure invalid	SKL-Y	0x0000021
	instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide	SKL-U	0x00000021
	for further details. Note: This setting should be set to '0' if there are not Invalid instructions.	SKL-H	0x00000021
		SKL-S	0x0000021
	Invalid Instruction 1 - This setting allows the customer to configure invalid	SKL-Y	0x00000042
	instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide	SKL-U	0x00000042
	for further details. Note: This setting should be set to '0' if there are not Invalid	SKL-H	0x00000042
	instructions.	SKL-S	0x00000042
	Invalid Instruction 2 - This setting allows the customer to configure invalid	SKL	0x0000060
	instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide	SKL-II	0x00000060
	for further details. Note: This setting should be set to '0' if there are not Invalid	SKL-U	0x00000060
	instructions.	SKL-H	0x00000060
		SKL-S	0x0000060
	Invalid Instruction 3 - This setting allows the customer to configure invalid	SKL-Y	0x000000AD
	for further details. Note: This setting should be set to '0' if there are not Invalid instructions.	SKL-U	0x000000AD
		SKL-H	0x000000AD
		SKL-S	0x000000AD
	Invalid Instruction 4 - This setting allows the customer to configure invalid	SKL-Y	0x00000B7
	for further details. Note: This setting should be set to '0' if there are not Invalid instructions.	SKL-U	0x00000B7
		SKL-H	0x00000B7
		SKL-S	0x00000B7
	Invalid Instruction 5 - This setting allows the customer to configure invalid	SKL-Y	0x00000B9
	instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide	SKL-U	0x00000B9
	instructions	SKL-H	0x00000B9
		SKL-S	0x00000B9
	Invalid Instruction 6 - This setting allows the customer to configure invalid instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide for further details. Note: This setting should be set to '0' if there are not Invalid instructions.	SKL-Y	0x00000C4
		SKL-U	0x00000C4
		SKL-H	0x00000C4
		SKL-S	0x00000C4
	Invalid Instruction 7 - This setting allows the customer to configure invalid	SKL-Y	0x00000C7
	instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide	SKL-U	0x00000C7
	for further details. Note: This setting should be set to '0' if there are not Invalid instructions.	SKL-H	0x00000C7
		SKL-S	0x00000C7
	Quad I/O Read Enabled	SKL-Y	No
	Values: Yes/No - This setting allows the customer to enable support for Ouad I/O	SKL-U	No
	Read capabilities for flash components. See Skylake H / LP SPI Programming guide	SKL-H	No
	for further details.	SKL-S	No
	Quad Qutput Read Enabled	SKI-Y	Yes
	Values: Yes/No - This setting allows the customer to enable support for Ouad	SKL-U	Yes
	Output Read capabilities for flash components. See Skylake H / LP SPI Programming	SKL-H	Yes
	guide for further details.	SKL-S	Ves
	Dead LD and Dead Status alook frequency		100
	Reau ID and Read Status Clock II equeficy	SKL-T	
	Values: 1/MHz, 30MHz, 48MHz - This setting allows the customer to configure the flash component clock frequency setting for Read ID and Read Status. See Skylake H		
			1/MHZ
		SKL-S	i / MHZ


Table 2-4. Intel[®] FIT - Flash Settings (Sheet 6 of 7)

#		Parameter		Platform	Settings
	Write and Erase Values: 17MHz, 3 flash component c Programming guid	clock frequency 30MHz, 48MHz - This setting lock frequency setting for Writ le for further details.	allows the customer to configure the e and Erase. See Skylake H / LP SPI	SKL-Y SKL-U SKL-H SKL-S	48MHz 48MHz 48MHz 48MHz
ick or	n Flash Settings in	the left tabs menu> VSCC	Table is expanded by default:	JKL-3	4010112
• v	SCC Table	2			
ATF2	26DF321			9 🗄	Add VSCC Entry
- 1	VSCC Entry 8				
	Parameter	Value	Help	Text	
VsccE	EntryName	ATF26DF321			
Vendo	or ID	0x1F			
Device	e ID 0	0x47	-		
Davice	ID 1	0×00			
Device		0000			
#		Parameter		Platform	Settings
	ATF26DF321 VSCC Entry				
8					
	Name - This settin component being flash component c	ng allow the OEM input a namused. Note: This is a free forn peration.	e designation for each flash n entry field it does not affect actual	SKL-Y SKL-U SKL-H SKL-S	Winbond Winbond Winbond Winbond
	Vendor ID - This component. See S	configures the JEDEC vendor kylake H / LP SPI Programmir	specific byte ID of the SPI flash g guide for further details.	SKL-Y SKL-U SKL-H SKL-S	OxEF OxEF OxEF OxEF
	Device ID 0 - Thi component. See S	is configures the JEDEC device kylake H / LP SPI Programmir	specific byte ID 0 of the SPI flash g guide for further details.	SKL-V SKL-U SKL-H SKL-S	0x40 0x40 0x40 0x40 0x40
	Device ID 1 - Thi component. See S	is configures the JEDEC device kylake H / LP SPI Programmir	specific byte ID 1 of the SPI flash g guide for further details.	SKL-Y SKL-U SKL-H SKL-S	0x18 0x18 0x18 0x18 0x18
9	+ Add VSCC Entr	у			

Г



Table 2-4. Intel[®] FIT - Flash Settings (Sheet 7 of 7)

Click on Flash Settings in the left tabs menu> SPI based RPMC Configuration is expanded by default:

10

SPI based RPMC Configuration

	Parameter	Value		Help Text	Help Text	
SPI base	ed RPMC Supported					
RPMC R	Rebind Enabled	No	-			
#		Parameter		Platform	Settings	
	SPI based RPMC Conf	iguration				
10						
	SPI based RPMC Supp	oorted		SKL-Y	No	
	Values: Yes/No - This	setting configures SPI based Replay	Protected Monotonic	SKL-U	No	
	Counter support. Note:	This setting only has effect when SI	PI part(s) supporting this	SKL-H	No	
	feature are used. Consu feature.	It SPI vendor data sheets to determ	ine support for this	SKL-S	No	
	RPMC Rebind Enabled			SKL-Y	No	
	Values: Yes/No - This	setting determines if RPMC rebindir	ng is allowed. Note: This	SKL-U	No	
	setting only has effect w	hen the SPI part(s) support this fea	ature are used.	SKL-H	No	
				SKL-S	No	
Click on	Flash Settings in the le	eft tabs menu> BIOS Configurat	ion is expanded by defa	ault:		
• [Bios Configuration	11 Value		Help Tex	1	
	I alameter	Value		Tieth Iev		
Top S	wap Block Size	64KB	-			
#		Parameter		Platform	Settings	
	BIOS Configuration			SKL-Y	64KB	
	Top Swap Block Size			SKL-U	64KB	
	Values: 64KB, 128KB,	256KB, 512KB, 1MB - This config	ures the Top Swap Block	SKL-H	64KB	
	EDS.	r Turther details see Skylake H / LP	Platform Controller Hub	SKL-S	64KB	



Table 2-5. Intel[®] FIT - Intel[®] ME Kernel (Sheet 1 of 5)

 Proces 	ssor	0			
Pa	arameter	Value	Help Te	xt	
Processor Err	nulation	No Emulation	-		
Missing Proce	essor Detection Aler	t No	-		
#		Parameter		Platform	Settings
Inte	el® ME Kernel -	Processor			
Proc Valu EMU EMU	cessor Emulatio ues: No Emulati JLATE Intel® vF JLATE Intel® Co	on on Pro (TM) capable Processor ore (TM) branded Processor		SKL-Y SKL-U SKL-H	No Emulation No Emulation EMULATE Intel® vPro (TM) capabl Processor
EML EML EML This Set t prod is ne Intel	JLATE Intel® Ce JLATE Intel® Pe JLATE Intel® Xe JLATE Intel® Xe setting determin this parameter to luction. This field eccessary to set th @ AMT.	eleron (R) branded Processo entium (R) branded Processo eon (R) branded Processo eon (R) branded Processor eon (R) Manageability capat es processor type to be emulat the type of processor that the will emulate that processor cla is to Emulate Intel® vPro™ Pro	or or ble Processor ted on pre-production silicon. target system will use during ss for pre-production silicon. It pocessor in order to enable	SKL-S	EMULATE Intel® vPro (TM) capabl Processor
Miss Valu enat the p	sing Processor I ues: Yes/No - Ti bled on Desktop / blatform has the	Detection Alert nis setting determines if missin ' Workstation platforms. Note: appropriate glue logic present.	g processor detection is This feature will only work if	SKL-Y SKL-U SKL-H SKL-S	NA NA No No
 Intel (R)) ME Firmware	Update 2	ME Firmware Update is exp	anded by defa	ult:
Par	ameter	Value	Help Text		
irmware Upda	te OEM ID	0000000-0000-0000-0000-000			
' lide MEBx Fir	mware Update	No -			
ntel(R) ME Re	, gion Flash Prot	Yes -			
#		Parameter		Platform	Settings
2 Inte	el® ME Kernel -	Intel® ME Firmware Update	3		
Firm to er of th	nware Update O nsure that custon ne platform.	EM ID - This setting allows cor hers can only update their platf	figuration of an OEM unique ID orm with images from the OEM	SKL-Y SKL-U SKL-H SKL-S	0 string 0 string 0 string 0 string
Hide Valu optic	e Intel® MEBx F Jes: Yes/No - Th Ion in the Intel® N	Firmware Update Control nis setting allows the customer MEBx interface.	to hide the Firmware Update	SKL-Y SKL-U SKL-H	No No



Table 2-5. Intel[®] FIT - Intel[®] ME Kernel (Sheet 2 of 5)

#		Parameter		Platform	Settings
	Intel® ME Region	Flash Protection Override	e	SKL-Y	Yes
	Values: Yes/No - 1	This setting enables descript	or unlock of the Intel® ME Region	SKL-U	Yes
	when the HMRFPO m	nessage is sent to firmware	prior to BIOS End of POST.	SKL-H	Yes
				SKL-S	Yes
Click or	n Intel® ME Kernel i	n the left tabs menu> In	tel® ME Services Configuration is	s expanded by	default:
▼ Int	tel (R) Services Con	figuration 3			
	Parameter	Value	Help Text		
ODM ID	used by Intel(R) Servi	0x0000000	-		
System	Integrator ID used by I	0x0000000	-		
Reserve	d ID used by Intel(R) S	0×0000000	-		
#		Parameter		Platform	Settings
	Intel® ME Kernel	- Intel® Services Configu	ration		
3					
	ODM ID used by Ir	ntel® Services - This settin	ng is for entering the ODM ID for	SKL-Y	0x0000000
	deperated by or regi	stered with Intel® Services	Web servers	SKL-U	0x0000000
	generated by or regi	stered with micro services		SKL-H	0x0000000
				SKL-S	0x0000000
	System Integrator	ID used by Intel® Service	ces - This setting is for entering the	SKL-Y	0x0000000
	System Integrator II	D for Intel® Services to ider	ntify the System Integrator. Note:	SKL-U	0x0000000
	This ID is either gen	erated by or registered with	The web services web servers.	SKL-H	0x0000000
				SKL-S	0x0000000
	Reserved ID used	by Intel® Services - This:	setting is for entering the Reserved	SKL-Y	0x0000000
	ID for Intel® Service	es currently not used.		SKL-U	0x0000000
				SKL-H	0x0000000
				SKL-S	0x00000000
Click on	Intel® ME Kernel i	n the left tabs menu> Im	nage Identification is expanded b	y default:	L
▼ Im	age Identification	4			
	Parameter	Value	Help Text		
OFM T	-	00000000			
UEINI Ta	g	0x000000	-		
#	1	Parameter		Platform	Settings
	Intel® ME Kernel -	 Image Identification 			
4		-			
	OEM Tag - This is a	free form 32bit field that all	ows the OEM to configure their own	SKL-Y	0x0000000
	unique identifier in t	he firmware image.		SKL-U	0x0000000
				SKL-H	0x00000000
				SKL-S	0x0000000



Table 2-5. Intel[®] FIT - Intel[®] ME Kernel (Sheet 3 of 5)

Click o	n Intel® ME Kerne	I in the left tabs men	nu> MCTP C	onfiguration is expanded by	y default:	
▼ MC	TP Configuration	n 5				
	Parameter	Value			Help Text	
MCTP S	tack Configuration	0x920030	De	efines the ME's 8-bits MCTP Endpo	int IDs for each SM	1Bus physical interface
MctpEsp	viEnabled	No	-			
MctpDev	vicePortEc	0x02	-			
MctpDev	vicePortSio	0x00	-			
MctpDev	vicePortIsh	0x00	-			
MctpDev	vicePortBmc	0x00	-			
#		Parar	imeter		Platform	Settings
5	MCTP Stack Conf Defines the Intel® interface (SMBus, communicate with means not used, a	Figuration ME's 8-bits MCTP Endr SMLink0, and SMLink1) MCTP end points. For e nd values 0xFF or 0x01	Ipoint ID's for I). These valu each of these 1 - 0x07 or 0	each SMBus physical les are needed for FW to a 3 bytes, a value of 0x00 x20 - 0x2F are not allowed.	SKL-Y SKL-U SKL-H SKL-S	0x920030 0x920030 0x920030 0x920030
	MctpEspiEnabled Value: Yes/No	I			SKL-Y SKL-U SKL-H SKL-S	No No No
	MctpDevicePortE	ic .			SKL-Y SKL-U SKL-H SKL-S	0x0 0x0 0x0 0x0 0x0
	MctpDevicePortS	Sio			SKL-Y SKL-U SKL-H SKL-S	0x00 0x00 0x00 0x00
	MctpDevicePortI	sh			SKL-Y SKL-U SKL-H SKL-S	0x00 0x00 0x00 0x00 0x00
	MctpDevicePortE	Bmc			SKL-Y SKL-U SKL-H SKL-S	0x00 0x00 0x00 0x00 0x00

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Table 2-5. Intel[®] FIT - Intel[®] ME Kernel (Sheet 4 of 5)

	irmware Diagnostics	6			
	Daramatar	Value	Help Tex	đ	
Automa	atic Built in Self Test	Disabled -		a	
#		Parameter		Platform	Settings
	Intel® ME Kernel - I	Firmware Diagnostics			-
6					
	Automatic Built in S	elf Test		SKL-Y	Disabled
	Values: Enabled/Dis	sabled ne firmware Automatic Built in	Self Test which is executed	SKL-U SKL-H	Disabled Disabled
	during first platform b	oot after initial image flashing.		SKL-S	Disabled
lick or	n Intel® ME Kernei in 	the left tabs menu> Inter®	Network Frame Forwarder	Configuration	is expanded by
	Parameter	Value	H	lelp Text	
ntel(R)	Network Frame Forwar	Yes	-		
		Feeblad	This cotting allows OEMs to dat	armina tha initial	
ntel(R)	Network Frame Forwar	Endbleu	This setting allows OEMS to de	termine the mittal	power-up state to
ntel(R) #	Network Frame Forwar	Parameter	This setting allows dens to der	Platform	power-up state to Settings
ntel(R) # 7	Network Frame Forwar	Parameter Ime Forwarder Configuratio	n	Platform	Settings
# 7	Network Frame Forwar	Parameter Ime Forwarder Configuratio me Forwarder Supported	n	Platform SKL-Y	Settings Yes
# 7	Intel® Network Fra Intel® Network Fra Values: Yes/No	Parameter Ime Forwarder Configuration me Forwarder Supported	n	Platform SKL-Y SKL-U	Yes
ntel(R) # 7	Intel® Network Fra Intel® Network Fra Values: Yes/No Note: Some SPT-H ma	Parameter Ime Forwarder Configuration me Forwarder Supported ay not support enabling of this	option.	Platform SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
ntel(R) #	Intel® Network Fra Intel® Network Fra Values: Yes/No Note: Some SPT-H ma Intel® Network Fra	Parameter Ime Forwarder Configuratio me Forwarder Supported ay not support enabling of this me Forwarder Initial Power	on Up State	Platform SKL-Y SKL-U SKL-H SKL-S SKL-Y	Yes Yes Yes Yes Yes Enabled
7	Intel® Network Fra Intel® Network Fra Values: Yes/No Note: Some SPT-H ma Intel® Network Fra Values: Enabled/Dis This setting allows OF	Parameter Ime Forwarder Configuration me Forwarder Supported ay not support enabling of this me Forwarder Initial Power sabled	on 	Platform SKL-Y SKL-U SKL-H SKL-S SKL-S SKL-Y SKL-U SKL-U SKL-U SKL-U	Yes Yes Yes Yes Enabled Enabled Enabled
7	Intel® Network Fra Intel® Network Fra Values: Yes/No Note: Some SPT-H ma Intel® Network Fra Values: Enabled/Dis This setting allows OEL Frame Forwarder feature	Parameter me Forwarder Configuratio me Forwarder Supported ay not support enabling of this me Forwarder Initial Power sabled Vis to determine the initial pow ure.	on - option. Up State ver up state for Intel® Network	Platform SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-U SKL-H SKL-S	Yes Yes Yes Yes Enabled Enabled Enabled Enabled
ilick or	Intel® Network Fra Intel® Network Fra Values: Yes/No Note: Some SPT-H ma Intel® Network Fra Values: Enabled/Dis This setting allows OEI Frame Forwarder feature Intel® ME Kernel in	Parameter ame Forwarder Configuration me Forwarder Supported ay not support enabling of this me Forwarder Initial Power sabled Vis to determine the initial power are. the left tabs menu> Post M	on coption. Up State ver up state for Intel® Network	Platform SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-Y SKL-U SKL-U SKL-H SKL-H SKL-S SKL-H	Yes Yes Yes Yes Yes Enabled Enabled Enabled Enabled
ilick or	Intel® Network Fra Intel® Network Fra Values: Yes/No Note: Some SPT-H ma Intel® Network Fra Values: Enabled/Dis This setting allows OEI Frame Forwarder feature Intel® ME Kernel in Post Manufacturin	Parameter ame Forwarder Configuration me Forwarder Supported ay not support enabling of this me Forwarder Initial Power sabled Vis to determine the initial power re. the left tabs menu> Post M Ig Lock	on coption.	Platform SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-U SKL-H SKL-H SKL-S Jed by default :	Yes Yes Yes Yes Yes Enabled Enabled Enabled Enabled
Tick or	Intel® Network Fra Intel® Network Fra Values: Yes/No Note: Some SPT-H ma Intel® Network Fra Values: Enabled/Dis This setting allows OEI Frame Forwarder feature In Intel® ME Kernel in Post Manufacturin Parameter	Parameter ame Forwarder Configuration me Forwarder Supported ay not support enabling of this me Forwarder Initial Power sabled Vis to determine the initial power are. the left tabs menu> Post M Ig Lock	on coption.	Platform Platform SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-U SKL-H SKL-S ded by default: Help Tet	power-up state fr Settings Yes Yes Yes Enabled Enabled Enabled Enabled



Table 2-5. Intel[®] FIT - Intel[®] ME Kernel (Sheet 5 of 5)

#		Parameter		Platform	Settings
	Intel® Post Manufactu	iring Lock			
8					
					Ne
	Parameter Intel® Post Manufacturing Lock Post Manufacturing NVAR Configuration Enabled Values: Yes/No This setting determines if modifications to Customer configurable NVARs is to be allowed after close of manufacturing. on Intel® ME Kernel in the left tabs menu> Reserved is expanded by default: Reserved 9 Parameter Value erved No Parameter Intel® ME Kernel - Reserved Reserved S		SKL-Y	No	
		SKL-U	No		
	allowed after close of ma	inufacturing.	e nvaks is to be	SKL-II	No
Click o	n Intel® MF Kernel in th	e left tabs menus Reserved is expa	nded by default.	SILE S	110
_					
•	Reserved	9			
_	Reserved	9			
-	Reserved	9 Maha		11-1- T	
	Parameter	9 Value		Help T	ext
Rese	Parameter	9 Value No	-	Help T	ext
Rese	Parameter erved	9 Value No	-	Help T	ext
Rese	Parameter erved	9 Value No Parameter	-	Help T	ext Settings
Rese	Parameter erved	9 Value No Parameter served	-	Help T	ext Settings
Rese #	Parameter erved Intel® ME Kernel - Res	9 Value No Parameter served	-	Help T	ext Settings
Rese #	Parameter erved Intel® ME Kernel - Res	9 Value No Parameter served	-	Help T	ext Settings
#	Parameter erved Intel® ME Kernel - Res	9 Value No Parameter served	-	Help T	ext Settings
#	Reserved Parameter erved Intel® ME Kernel - Reserved Reserved	9 Value No Parameter Served	-	Help T Platform SKL-Y	Settings
#	Reserved Parameter erved Intel® ME Kernel - Res Reserved Values: Yes/No	9 Value No Parameter Served	-	Help T Platform SKL-Y SKL-U	Settings No No
#	Reserved Parameter erved Intel® ME Kernel - Reserved Reserved Values: Yes/No	9 Value No Parameter served	-	Help T Platform SKL-Y SKL-U SKL-H	ext Settings No No No

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Table 2-6. Intel[®] FIT - Intel[®] AMT (Sheet 1 of 7)

Click on Intel® AMT in the left Intel(R) AMT Config 	tabs menu> Intel® AMT is	s expanded by default:		
Parameter	Value		Help	Fext
Intel(R) AMT Supported	Yes	This setting allows	customers to di	sable Intel(R) AMT on
Intel(R) ME Network Services S	Yes	This setting allows	customers to er	hable / disable Intel(R)
Manageability Application Supp	Yes	This setting allows	customers to pe	ermenantly disable Int
Manageability Application initial	Enabled	This setting allows	customers to de	termine the power up
Intel(R) AMT Idle Timeout	0xFFFF	This setting configu	res the idle time	eout value before Inte
Intel(R) AMT Watchdog Autom	No	This setting allows	customers to er	able the Intel (R) ME
#	Parameter		Platform	Settings
Intel® AMT Supported Values: Yes/No - This s platform and force the pl setting has been set to d descriptor has been locke Intel® ME Network Se Values: Yes/No - This s Network Services on the will also be disabled	etting allows customers to di atform into Standard Manage isabled Intel® AMT cannot be d. This setting applies to Des rvices Supported setting allows customers to e platform. Note: If this settin	isable Intel® AMT on the ability mode. Note: If this e re-enabled once the sktop and Workstation only. nable / disable Intel® ME g is disabled Intel® AMT	SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-U	Yes Yes Yes Yes Yes Yes Yes
Intel® Manageability / Values: Yes/No - This s platforms to operate in S applies to Desktop and W	Intel® Manageability Application Supported Values: Yes/No - This setting allows customers to force Intel® AMT enabled platforms to operate in Standard Manageability mode. Note: This setting only applies to Desktop and Workstation platforms. Manageability Application initial power-up state Values: Enabled/Disabled This setting allows customers to determine the power up state for Intel® AMT or Standard Manageability. Note: If this setting is disabled Intel® AMT or Standard Manageability can still be re-enabled through the Intel® MEBx interface.		SKL-S SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes Yes
Manageability Applicat Values: Enabled/Disat This setting allows custor Standard Manageability. Manageability can still be			SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
Intel® AMT Idle Timeout Values: 0xFFFF - This setting configures the idle AMT enters into an off state.		eout value before Intel®	SKL-Y C SKL-U C SKL-H C	OxFFFF OxFFFF OxFFFF OxFFFF
Intel® AMT Watchdog	Automatic Reset Enabled		SKL-Y	No
Values: Yes/No - This s firmware to trigger an au Presence are in a hung s when the watchdog expir re-armed for reuse via m	etting allows customers to en tomatic platform reset if eith tate. Note: This feature only es. After this feature has trig anagement console.	nable the Intel® ME ler the MEI or Agent allows one reset at a time gered a reset, it must be	SKL-U SKL-H SKL-S	No No No



Table 2-6. Intel[®] FIT - Intel[®] AMT (Sheet 2 of 7)

	VM Configuration		iguration is expanded by der			
	Parameter	Value	Help T	ext		
rmwa	re KVM Screen Blanking	No	-			
/M R	edirection Supported	Yes	-			
¥		Parameter		Platform	Set	tings
2	Intel® AMT - KVM	Configuration				
	Firmware KVM Scr Values: Yes/No - T firmware image. No	een Blanking This setting enables KVM Scre te: This feature is dependent	een blanking capabilities in the on processor level support.	SKL-Y SKL-U SKL-H SKL-S	No No No No	
	KVM Redirection S Values: Yes/No - T Redirection capabilit disabled it cannot be	upported This setting allows OEMs to er ies of the firmware. Note: If e re-enabled once the descrip	hable / disable the KVM this setting has been set to tor has been locked.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes	
P	rovisioning Configu	ration 3		u by delaun.		
	Parameter	Value	Help T	ext		
mbed	ded Host Based Config	No	-			
KI Do	main Name Suffix		-			
#		Parameter		Platform	Set	tings
3	Intel® AMT - Prov	isioning Configuration				
	Embedded Host Ba	ased Configuration		SKL-Y	No	
	Values: Yes/No - T Host Based Configur embedded systems a appropriate for busir	This setting allows customers ation. Important - EHBC is pr as it offers less user privacy/s ness client systems.	to enable / disable Embedded rimarily intended for use in security protection than may be	SKL-U SKL-H SKL-S	No No No	
	Note: The Intel® FI based on selection h	T tool will not adjust the Red ere. Please set security level	irection Privacy/Security value as needed.			
	PKI Domain Name Domain Name Suffix For normal out-of-bo	Suffix - This setting allow O used for PKI provisioning in px provisioning functionality th	EMs to pre-configure the their firmware image. Note: nis setting should be left empty.			



Table 2-6. Intel[®] FIT - Intel[®] AMT (Sheet 3 of 7)

Click or	n Intel® AMT in the	e left tabs menu> OEM Cus	stomizable Certificate 1 is exp	anded by defau	ult:
▼ 0E	M Customizable Certif	icate 1			
	Paramotor	Value	Help Te	vt	
Certificat	te Enabled	No	This setting allows customers to ena	ble PKI provisionin	g Custo
Certificat	te Friendly Name		This setting allows customers to ass	ion a user friendly	name for
Certificat	te Stream		This setting allows customers to input	ut hash stream for I	PKI provi
#	1	Parameter		Platform	Settings
	Intel® AMT - OEM	A Customizable Certificate	1		
4					
	Certificate Enable Values: Yes/No - Custom Certificate	e d This setting allows customers 1.	s to enable PKI provisioning	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Certificate Friend friendly name for P characters.	Ily Name - This setting allows KI provisioning Custom Certif	s customers to assign a user ficate 1. Maximum of 32		
	Certificate Strear provisioning Custor addition to those al If the platform is u	n - This setting allows custom n Certificate 1. If enabled the ready pre-loaded in base firm n-configured the Custom Cert	ers to input hash stream for PKI e certificate will be used in ware during provisioning. Note: tificate Hash will be deleted.		
Click or	n Intel® AMT in the	e left tabs menu> OEM Cus	stomizable Certificate 2 is exp	anded by defau	ult:
▼ 0E	M Customizable Certi	ficate 2 5			
	Parameter	Value	Help Te	ext	
Certifica	te Enabled	No	This setting allows customers to ena	able PKI provisionin	g Custo
Certificat	te Friendly Name		This setting allows customers to ass	sign a user friendly	name for
Certificat	te Stream		This setting allows customers to inp	ut hash stream for	PKI provi
#		Parameter		Platform	Settings
5	Intel® AMT - OEM	/ Customizable Certificate	2		
	Certificate Enable	ed		SKL-Y	No
	Values: Yes/No - Custom Certificate	This setting allows customers 2.	s to enable PKI provisioning	SKL-U SKL-H	No
				SKL-S	No
	Certificate Friend friendly name for P characters.	Ily Name - This setting allow: KI provisioning Custom Certif	s customers to assign a user ficate 2. Maximum of 32		
	Certificate Strear provisioning Custor addition to those al If the platform is u	n - This setting allows custom m Certificate 2. If enabled the ready pre-loaded in base firm n-configured the Custom Cert	ers to input hash stream for PKI e certificate will be used in ware during provisioning. Note: tificate Hash will be deleted.		



Table 2-6. Intel[®] FIT - Intel[®] AMT (Sheet 4 of 7)

Click or	n Intel® AMT in the	left tabs menu> OEM Custo	omizable Certificate 3 is exp	anded by defau	ult:	
▼ OE	EM Customizable Certifi	cate 3 6				
	Parameter	Value	Help T	ext		
Certifica	ate Enabled	No	This setting allows customers to er	o enable PKI provisioning Custo		
Certifica	ate Friendly Name		This setting allows customers to as	sign a user friendly	name for	
Certifica	ate Stream		This setting allows customers to in	put hash stream for	r PKI provi	
#		Parameter		Platform	Set	ings
	Intel® AMT - OEM	Customizable Certificate 3				-
6						
	Certificate Enabled	I 		SKL-Y	No	
	Custom Certificate 3.	his setting allows customers f	to enable PKI provisioning	SKL-U SKL-H	No No	
				SKL-S	No	
	Certificate Friendly friendly name for PKI	Name - This setting allows of provisioning Custom Certification	customers to assign a user ate 3. Maximum 32 characters.			
	Certificate Stream provisioning Custom addition to those alre If the platform is un-	 This setting allows customer Certificate 3. If enabled the c ady pre-loaded in base firmw. configured the Custom Certifi 	rs to input hash stream for PKI certificate will be used in are during provisioning. Note: icate Hash will be deleted.			
▼ OE	EM Default Certificate 1	7				
	Parameter	Value	Help T	ext		
Certifica	ate Enabled	No	This setting allows customers to en	able PKI provisioni	ng Default	
Certifica	ate Friendly Name		This setting allows customers to as	sign a user friendly	name for	
Certifica	ate Stream		This setting allows customers to in	out hash stream for	PKI provi	
#		Parameter		Platform	Set	ings
7	Intel® AMT - OEM	Default Certificate 1				
	Certificate Enabled			SKL-Y	No	
	Values: Yes/No - T Default certificate 1.	his setting allows customers t	to enable PKI provisioning	SKL-U SKL-H	No No	
<u>.</u>				SKL-S	No	
	Certificate Friendly friendly name for PK	Name - This setting allows of provisioning Default Certification	customers to assign a user ate 1. Maximum 32 characters.			
	Certificate Stream provisioning custom used in addition to th Unlike Customizable the platform is up or	- This setting allows customer certificate 1. Note: Default C nose already pre-loaded in firr Certificates the Default Certif ovisioned	rs to input hash stream for PKI ertificates if enabled will be mware during provisioning. icates are not deleted when			



Table 2-6. Intel[®] FIT - Intel[®] AMT (Sheet 5 of 7)

lick or	n Intel® AMT in the I	eft tabs menu> OEM Defa	ult Certificate 2 is expanded	by default:		
▼ 0	EM Default Certificate 2	8				
	Parameter	Value	Help T	ext		
Certifica	ate Enabled	No	This setting allows customers to en	enable PKI provisioning Default		
Certifica	ate Friendly Name		This setting allows customers to as	sign a user friendly	name for	
Certifica	ate Stream		This setting allows customers to in	out hash stream for PKI provi		
#		Parameter		Platform	Sett	ings
	Intel® AMT - OEM I	Default Certificate 2				
8						
	Certificate Enabled			SKL-Y	No	
	Values: Yes/No - The Default certificate 2.	nis setting allows customers	to enable PKI provisioning	SKL-U SKL-H	NO NO	
				SKL-S	No	
	Certificate Friendly friendly name for PKI	Name - This setting allows provisioning Default Certific	customers to assign a user ate 2. Maximum 32 characters.			
	Certificate Stream provisioning custom of used in addition to th Unlike Customizable the platform is un-pro	 This setting allows custome certificate 2. Note: Default C iose already pre-loaded in fir Certificates the Default Certif ovisioned. 	rs to input hash stream for PKI certificates if enabled will be mware during provisioning. ficates are not deleted when			
▼ OE	EM Default Certificate 3	9	· · ·	-		
	Parameter	Value	Help T	ext		
ertifica	te Enabled	No	This setting allows customers to en	able PKI provisioni	ng Default	
ertifica	te Friendly Name		This setting allows customers to as	sign a user friendly	/ name for	
ertifica	ate Stream		This setting allows customers to in	put hash stream for	r PKI provi	
#		Parameter		Platform	Sett	ings
9	Intel® AMT - OEM I	Default Certificate 3				
	Certificate Enabled			SKL-Y	No	
	Values: Yes/No - The Default certificate 3.	his setting allows customers	to enable PKI provisioning	SKL-U SKL-H	No No	
				SKL-S	No	
	Certificate Friendly friendly name for PKI	Name - This setting allows provisioning Default Certific.	customers to assign a user ate 3. Maximum 32 characters.			
	Certificate Stream provisioning custom of used in addition to th Unlike Customizable	- This setting allows custome certificate 3. Note: Default C lose already pre-loaded in fir Certificates the Default Certif pvisioned	rs to input hash stream for PKI Certificates if enabled will be mware during provisioning. ficates are not deleted when			



Table 2-6. Intel[®] FIT - Intel[®] AMT (Sheet 6 of 7)

Click on	Intel® AMT in the	left tabs menu> OEM Def	ault Certificate 4 is expanded	by default:		
▼ OEI	M Default Certificate 4	10				
	Parameter	Value	Help Te	ext		
Certificat	e Enabled	No	This setting allows customers to en	able PKI provisionin	g Default	
Certificat	e Friendly Name		This setting allows customers to as	sign a user friendly	name for	
Certificat	e Stream		This setting allows customers to inp	ut hash stream for l	PKI provi	
#		Parameter		Platform	Settings	
	Intel® AMT - OEM	Default Certificate 4				
10						
	Certificate Enable	d		SKL-Y	No	
	Values: Yes/No - Default certificate 4	This setting allows customers	s to enable PKI provisioning	SKL-U SKL-H	No No	
				SKL-S	No	
	Certificate Friendl friendly name for Pl	y Name - This setting allows (I provisioning Default Certif	s customers to assign a user icate 4.			
	Certificate Stream provisioning custom used in addition to t Unlike Customizable the platform is un-p	 This setting allows custom certificate 4. Note: Default hose already pre-loaded in f Certificates the Default Cert rovisioned. 	ers to input hash stream for PKI Certificates if enabled will be irmware during provisioning. tificates are not deleted when			
OEN	I Default Certificate 5	0	· · · · · · · · · · · · · · · · · · ·	-		
	Parameter	Value	Help Te	xt		
Certificate	Enabled	No	This setting allows customers to enal	ble PKI provisioning	Default	
Certificate	Friendly Name		This setting allows customers to assi	ssign a user friendly name for		
Certificate	e Stream		This setting allows customers to input	nput hash stream for PKI provi		
#		Parameter		Platform	Settings	
1	Intel® AMT - OEM	Default Certificate 5				
	Certificate Enabled			SKL-Y	No	
	Values: Yes/No - Default certificate 5	This setting allows customers	s to enable PKI provisioning	SKL-U SKL-H	No	
				SKL-S	No	
	Certificate Friendl friendly name for Pl	y Name - This setting allows (I provisioning Default Certif	s customers to assign a user icate 5.			
	Certificate Stream provisioning custom used in addition to t Unlike Customizable the platform is un-p	- This setting allows custom certificate 5. Note: Default hose already pre-loaded in f certificates the Default Cert rovisioned.	ers to input hash stream for PKI Certificates if enabled will be irmware during provisioning. tificates are not deleted when			



Table 2-6. Intel[®] FIT - Intel[®] AMT (Sheet 7 of 7)

Click or	n Intel® AMT in the	e left tabs menu> Red	lirection Configuration is expanded	by default:			
🔻 Re	direction Configura	ation 12					
	anoonon oonngan						
	Parameter Value Help Text						
Redirecti	rection Localized Language English This setting allows customers to configure				ed langu		
Redirecti	direction Privacy / Security Default This setting allows			figure the Privacy a	and Secu		
#		Parame	ter	Platform	Settings		
12	Intel® AMT - Red	irection Configuratior	1				
	Redirection Local which localized lang output information starts).	ized Language - This s juage will be used initial (Examples: May be disp	SKL-Y SKL-U SKL-H SKL-S	English English English English			
	Redirection Privacy / Security Level - This setting allows customers to configure the Privacy and Security level for redirection operations. Default enables all redirection ports (User consent is configurable). Enhanced - Enables all redirection ports. (User consent is required and cannot be disabled).				Default Default Default Default		
	Extreme - Disables Note: The Intel® F Configuration value needed.	Redirection and Remot IT tool will not adjust th based on selection here	e Configuration / Client Control Mode. he Embedded Host Based e. Please set EHBC to yes or no as				
Click or	n Intel® AMT in the	e left tabs menu> TLS	Configuration is expanded by defa	ault:			
▼ TL	S Configuration	13					
	Parameter	Value	Help Tex	d			
Transport	Transport Layer Security Supp Yes This setting allows customers to ena				re Trans		
13	Intel® AMT - TLS	Configuration					
#		Parame	ter	Platform	Settings		
	Transport Layer S Values: Yes/No - Transport Layer Sec permanently disable	Security Supported This setting allows custo curity support. Note: If ed in the firmware imag	omers to enable / disable firmware this is disabled TLS will be e.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes		



Table 2-7. Intel[®] FIT - Intel[®] Platform Protection (Sheet 1 of 4)

•	Content Protection	0					
	Parameter	Value		Help Tex	t		
PAV	AVP Supported Yes This setting determines if the Protected Audio Vide						
LSP	CON Internal Display Port 1	None	This setting deterr	This setting determines which port for LSPCON will be			
HDC	CP Internal Display Port 1 - 5	K None	This setting deterr	nines which port is	connected for 5		
HDC	CP Internal Display Port 2 - 5	K None	This setting deterr	nines which port is	connected for 5		
¥		Parameter		Platform	Settings		
	Platform Protection - Co	ontent Protection					
	PAVP Supported			SKL-Y	Yes		
	Values: Yes/No			SKL-U	Yes		
	This setting determines if	he Protected Audio Video	Path (PAVP) feature will be	SKL-H	Yes		
	permanently disabled in th	e FW image.		SKL-S	Yes		
	LSPCON Internal Displa	y Port 1 - LSPCON / 4K		SKL-Y	None		
	Values: None, Port B, Po	ort C, Port D		SKL-U	None		
	This setting determines wh	nich port for LSPCON will b	e connected to the HDCP 2.2	SKL-H	None		
	bridge adapter Display 1.			SKL-S	None		
	HDCP Internal Display F	Port 1 - 5K		SKL-Y	None		
	Values: None, Port A, Po	ort B, Port C, Port D		SKL-U	None		
	This setting determines wh Display 1.	hich port is connected for 5	5K output on the Internal	SKL-H SKL-S	None None		
	Note: Both Display Port 1 & 2 ne Intel® AMT KVM is not su	ed to be configured for pro oported if both HDCP Intern	oper operation. nal Display ports are used.				
	HDCP Internal Display F	Port 2 - 5K		SKL-Y	None		
	Values: None, Port A, Po	ort B, Port C, Port D		SKL-U	None		
	This setting determines wh	nich port is connected for 5	K output on the Internal	SKL-H	None		
	Display 2.			SKL-S	None		
	Note:	ad to be configured for pro	anor energian				
	Intel® AMT KVM is not sup	ported if both HDCP Inter	nal Display ports are used.				
k o	n Platform Protection in t	he left tabs menu> Gra	phics uController is expanded	ed by default:			
•	Graphics uController	2					
	Parameter	Value	Help T	ext			
Suc I	Encryption Key 00	00 00 00 00 00 00 00 00 00 00	This option is for entering the raw h	ash 256 bit string or cert	tifica		



Table 2-7. Intel[®] FIT - Intel[®] Platform Protection (Sheet 2 of 4)

#		Platform	Settings					
2	Platform Protection - Graphics UController							
Click o	GuC Encryption Key SKL-Y 0x0000000 Values: This option is for entering the raw hash 256 bit string or certificate file for the Graphics uController. SKL-U 0x0000000 SKL-H 0x0000000 0x0000000 0x00000000 SKL-S 0x0000000 0x00000000							
•	Hash Key Configurat	tion for Bootguard / ISH	3					
	Parameter	Value		Help Text				
OE	M Public Key Hash	00 00 00 00 00 00 00 00 00 00	This option is for en	tering the raw hash str	ing for Boot Guari			
#		Parameter		Platform	Settings			
3	Platform Protection - Hash Key Configuration for Bootguard / ISH							
	OEM Public Key Hash SKL-Y 0x0000000 Values: This option is for entering the raw hash string or certificate file for Boot SKL-U 0x0000000 Guard and ISH. This 256-bit field represents the SHA-256 hash of the OEM public key corresponding to the private key used to sign the BIOS-SM or ISH image. SKL-H 0x0000000 Please see Appendix F for further details. SKL-S 0x0000000							
	Boot Guard Configu	ration 4	onfiguration is exp	banded by default:				
	Parameter	Value		Help Text				
Кеу	Manifest ID	0x0	This option is for	entering the hash of a	nother public key			
Boo	t Guard Profile Configuration	Boot Guard Profile 0 - No_FVME	This option config	ures the which Boot G	uard Policy Profil			
CPU	J Debugging	Enabled	This setting deter	mines if CPU debug m	odes will be disp			
BSP	Initialization	Enabled	This setting deter	mines BSP behavior w	hen it receives a			
#	1		Platform	Settings				
4	Platform Protection - Boo	t Guard Configuration						
	Key Manifest ID Values: This option is for en ACM to verify the Boot Policy	SKL-Y SKL-U SKL-H SKL-S	0x0 0x0 0x0 0x0 0x0					



#		Parameter	Parameter		Settings
	Boot Guard Profile Configu	uration		SKL-Y	Boot Guard
	Values: Boot Guard Profile	≥ 0 - No_FVME			Profile 0 -
	Boot Guard Profile 1 - VE	-			No_FVME
	Boot Guard Profile 2 - VME	E		SKL-U	Boot Guard
	Boot Guard Profile 3 - VM		Profile U -		
	Boot Guard Profile 4 - FVE		Boot Guard		
	Boot Guard Profile 5 - FVM	SKL-H	Profile 0 -		
	This option configures which Boot Guard Policy Profile will be used.				No_FVME
	3			SKL-S	Boot Guard
					Profile 0 -
			NO_FVME		
	CPU Debugging	SKL-Y	Enabled		
	Values: Enabled/Disabled			SKL-U	Enabled
	This setting determines if CPU	U debug modes will be displayed	d. When set to	SKL-H	Enabled
	Enabled CPU debugging is e	nabled.		SKL-S	Enabled
	BSP Initialization			SKL-Y	Enabled
	Values: Enabled/Disabled			SKL-U	Enabled
	This setting determines BSP I	behavior when it receives an IN	IT signal. When set to	SKL-H	Enabled
	'Enabled' BSP will behave nor	mally if it receives an INIT (Disa	abled BSP Initialization	SKL-S	Enabled
	(DBI) BI(=0). when set to DI	sabled BSP will shutdown if it re	eceives an INIT ("DBI"		
ick o	n Platform Protection in the	left tabs menus Intel® PTT	Configuration is ever	anded by default	
•	Intel (R) PTT Configur	ation 5			
•	Intel (R) PTT Configur	ration 5 Value		Help Tex	t
Intel	Parameter (R) PTT Configur	ration 5 Value Enabled	This setting deter	Help Tex mines if Intel(R) PTT	t is enabled on pla
▼ Inte	Intel (R) PTT Configur	ration 5 Value Enabled Yes	This setting deten This setting perma	Help Tex mines if Intel(R) PTT anently disables Intel	t is enabled on plat (R) PTT in the firr
Inte Inte	Intel (R) PTT Configur	Tation 5 Value Enabled Yes Yes	This setting detern This setting perma This setting will pe	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In	t is enabled on plat (R) PTT in the firr tel(R) PTT throug
Inte Inte	Intel (R) PTT Configur	Tation 5 Value Enabled Yes Yes	This setting detern This setting perma This setting will pe	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In	t is enabled on pla (R) PTT in the firr tel(R) PTT throug
Inte Inte Inte	Intel (R) PTT Configur	Tation 5 Value Enabled Yes Yes Parameter	This setting detern This setting perma This setting will pe	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform	t is enabled on pla (R) PTT in the firr ttel(R) PTT throug Settings
Inte Inte Inte	Intel (R) PTT Configur Parameter I(R) PTT initial power-up state I(R) PTT Supported I(R) PTT Supported I(R) PTT Supported [FPF]	Value Enabled Yes Yes Parameter I® PTT Configuration	This setting detern This setting perma This setting will pe	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform	t is enabled on pla (R) PTT in the firr tel(R) PTT throug Settings
Inte Inte #	Intel (R) PTT Configur	Tation 5 Value Enabled Yes Yes Parameter I® PTT Configuration	This setting detern This setting perma This setting will pe	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform	t is enabled on pla (R) PTT in the firr tel(R) PTT throug Settings
Intel Intel Inte	Intel (R) PTT Configur	This setting determines if late	This setting detern This setting perma This setting will p	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform	t is enabled on plai (R) PTT in the firr ttel(R) PTT throug Settings
Intel Intel Intel #	Intel (R) PTT Configur	Value Enabled Yes Yes Parameter I® PTT Configuration Ip state - This setting determines if Interview	This setting detern This setting perma This setting will perma This setting will perma el® PTT is enabled on	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform SKL-V SKL-U SKL-U	t is enabled on plat (R) PTT in the firm tel(R) PTT throug Settings Enabled Enabled Enabled
#	Intel (R) PTT Configur Parameter I(R) PTT initial power-up state I(R) PTT Supported I(R) PTT Supported [FPF] Platform Protection - Inte Intel® PTT initial power-u Values: Enabled/Disabled platform power-up.	Value Enabled Yes Yes Parameter I® PTT Configuration Ip state - This setting determines if Interview	This setting detern This setting perma This setting will perma This setting will perma el® PTT is enabled on	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform SKL-Y SKL-U SKL-H SKL-H SKL-H	t is enabled on plat (R) PTT in the firr ttel(R) PTT throug Settings Enabled Enabled Enabled Disabled
#	Intel (R) PTT Configur Parameter I(R) PTT initial power-up state I(R) PTT Supported I(R) PTT Supported [FPF] Platform Protection - Inte Intel® PTT initial power-u Values: Enabled/Disabled platform power-up.	value Value Enabled Yes Yes Parameter I® PTT Configuration Ip state - This setting determines if Interview	This setting detern This setting perma This setting will perma el® PTT is enabled on	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform SKL-Y SKL-U SKL-H SKL-H SKL-S	t is enabled on plat (R) PTT in the firr ttel(R) PTT throug Settings Enabled Enabled Enabled Disabled
#	Intel (R) PTT Configur Parameter I(R) PTT initial power-up state I(R) PTT Supported I(R) PTT Supported [FPF] Platform Protection - Intel Intel® PTT initial power-u Values: Enabled/Disabled platform power-up. Intel® PTT Supported	value Value Enabled Yes Yes Yes Parameter I® PTT Configuration Ip state - This setting determines if Interview	el® PTT is enabled on	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform SKL-Y SKL-U SKL-H SKL-H SKL-S SKL-Y	t is enabled on pla (R) PTT in the firr ttel(R) PTT throug Settings Enabled Enabled Enabled Disabled Yes
#	Intel (R) PTT Configur Parameter I(R) PTT initial power-up state I(R) PTT Supported I(R) PTT Supported [FPF] Platform Protection - Intel Intel® PTT initial power-u Values: Enabled/Disabled platform power-up. Intel® PTT Supported Values: Yes/No - This settinimate	value Value Enabled Yes Yes Parameter I® PTT Configuration Ip state - This setting determines if Intermines if Intermines if Intermines if Intermines if Intermines if Intermines Intel®	el® PTT is enabled on	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-Y SKL-U SKL-Y	t is enabled on pla (R) PTT in the firr ttel(R) PTT throug Settings Enabled Enabled Enabled Disabled Yes Yes
#	Intel (R) PTT Configur Parameter I(R) PTT initial power-up state I(R) PTT Supported I(R) PTT Supported [FPF] Platform Protection - Inte Intel® PTT initial power-u Values: Enabled/Disabled platform power-up. Intel® PTT Supported Values: Yes/No - This settin image.	value Value Enabled Yes Yes Yes Parameter I® PTT Configuration Ip state - This setting determines if Intermines Intermines Intermines Intermines	el® PTT is enabled on PTT in the firmware	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-U SKL-H	t is enabled on pla (R) PTT in the firr tel(R) PTT throug Settings Enabled Enabled Enabled Disabled Yes Yes Yes
#	Intel (R) PTT Configur Parameter I(R) PTT initial power-up state I(R) PTT Supported I(R) PTT Supported [FPF] Platform Protection - Inte Intel® PTT initial power-u Values: Enabled/Disabled platform power-up. Intel® PTT Supported Values: Yes/No - This settin image.	value Value Enabled Yes Yes Yes Parameter I® PTT Configuration Ip state - This setting determines if Internet in the setting determines in the setting dete	el® PTT is enabled on PTT in the firmware	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-U SKL-H SKL-S	t is enabled on pla (R) PTT in the firr tel(R) PTT throug Settings Enabled Enabled Enabled Disabled Yes Yes Yes Yes Yes
#	Intel (R) PTT Configur Parameter I(R) PTT initial power-up state I(R) PTT Supported I(R) PTT Supported [FPF] Platform Protection - Intel Intel® PTT initial power-u Values: Enabled/Disabled platform power-up. Intel® PTT Supported Values: Yes/No - This setting image. Intel® PTT Supported [FPF]	Value Value Enabled Yes Yes Yes Parameter I® PTT Configuration Ip state - This setting determines if Internet in the setting determines in the	el® PTT is enabled on PTT in the firmware	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-Y SKL-Y	t is enabled on pla (R) PTT in the firr tel(R) PTT throug Settings Enabled Enabled Enabled Disabled Yes Yes Yes Yes Yes Yes
#	Intel (R) PTT Configur Parameter I(R) PTT initial power-up state I(R) PTT Supported I(R) PTT Supported [FPF] Platform Protection - Intel Intel® PTT initial power-u Values: Enabled/Disabled platform power-up. Intel® PTT Supported Values: Yes/No - This setting image. Intel® PTT Supported [FPF] Values: Yes/No - This setting Intel® PTT Supported [FPF] Intel® PTT Supported [Value Enabled Yes Yes Yes Parameter I® PTT Configuration Ip state - This setting determines if Internation ng permanently disables Intel® F] ng will permanently disable Intel	el® PTT through	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-Y SKL-U	t is enabled on pla (R) PTT in the firm tel(R) PTT throug Settings Enabled Enabled Enabled Disabled Yes Yes Yes Yes Yes Yes Yes
#	Intel (R) PTT Configur Parameter I(R) PTT initial power-up state I(R) PTT Supported I(R) PTT Supported I(R) PTT Supported [FPF] Platform Protection - Intel Intel® PTT initial power-up Values: Enabled/Disabled platform power-up. Intel® PTT Supported Values: Yes/No - This setting image. Intel® PTT Supported [FPF] Values: Yes/No - This setting platform FPFs. Caution: Using the platform berdware	value Value Enabled Yes Yes Parameter I® PTT Configuration Ip state - This setting determines if Intermines if Intermin	el® PTT is enabled on PTT in the firmware	Help Tex mines if Intel(R) PTT anently disables Intel ermanently disable In Platform SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-U SKL-H	t is enabled on plat (R) PTT in the firr tel(R) PTT throug Settings Enabled Enabled Enabled Disabled Yes Yes Yes Yes Yes Yes Yes Yes

Table 2-7. Intel[®] FIT - Intel[®] Platform Protection (Sheet 3 of 4)



Table 2-7. Intel[®] FIT - Intel[®] Platform Protection (Sheet 4 of 4)

Click on Platform Protection in the left tabs menu> TPM Over SPI Bus Configuration is expanded by default:

Parameter	Parameter Value		Help Text			
TPM Clock Frequency	17MHz	This setting deter	This setting determines the clock frequency setting t			
TPM Over SPI Bus Enabled	No	This setting deter	This setting determines if TPM over SPI bus is enabled			
ŧ	Parameter					
	Pri over SPI Bus configurat	ion				
TPM Clock Frequency			SKL-Y	17MHz		
	nes the clock frequency	SKL-U	17MHz			
Values: 17MHz, 30MHz	setting to be used for the TPM over SPI bus.					
Values: 17MHz, 30MHz setting to be used for the	TPM over SPI bus.		SKL-H	1710112		
Values: 17MHz, 30MHz setting to be used for the	TPM over SPI bus.		SKL-H SKL-S	17MHz		
Values: 17MHz, 30MHz setting to be used for the TPM Over SPI Bus Ena	bled		SKL-H SKL-S SKL-Y	17MHz No		
Values: 17MHz, 30MHz setting to be used for the TPM Over SPI Bus Ena Values: Yes/No - This s	bled blet over SPI bus.	PI bus is enabled on the	SKL-H SKL-S SKL-Y SKL-U	17MHz No No		
Values: 17MHz, 30MHz setting to be used for the TPM Over SPI Bus Ena Values: Yes/No - This s platform.	bled betting determines if TPM over S	PI bus is enabled on the	SKL-H SKL-S SKL-Y SKL-U SKL-H	17MHz No No No		



Table 2-8. Intel[®] FIT - Integrated Clock Controller (Sheet 1 of 13)

Click or default	n Integrated Clock	Controller in the lef	t tabs menu> Integrated Clock	Controller Poli	cies are expar	nded by
 Inte 	grated Clock Con	troller Policies	1			
	Parameter	Value	Hel	p Text		
Register L	ock Policy	0:Default	Policy applied to ICC Registers a	s at EOP.		
Boot Profi	le	Profile 0 Profile applied during each boot.				
Failsafe B	loot Profile	Profile 0	Boot profile used when system in	stability is detected		
Profile Cha	angeable	true	Allows user to change boot profile	e via BIOS menu or 3	3rd party appli	
#		Paramet	er	Platform	Sett	ings
1	Integrated Clock	< Controller - Integra	ted Clock Controller Policies			
	Register Lock Po	olicy		SKL-Y	0: Default	
	Values: 0:Defaul	It, 1:All Locked, 2: All	Unlocked	SKL-U	0: Default	
	registers left acces	ntrois Register lock poli ssible to host after EOP.	cy. It defines the integrated clock	SKL-H SKL-S	0: Default	
	0:Default - Locks clock frequency ar	all but the registers as and spread settings.	sociated to adjust BCLK nominal	SKE'S	0. Delaut	
	1:All Locked - Lo to these registers	ocks all integrated clock via Intel® ME Firmware	registers and disables all writes e.			
	2:All Unlocked - option is mainly	Leaves pre-EOP integra used for debug purp	ited clock registers unlocked. This ose.			
	Double click on va options.	lue column of this para	meter to choose from available			
	Boot Profile			SKL-Y	Profile 0	
	This parameter all	owe upor to coloct dofo	ult profile to be used by the final	SKL-U	Profile 0	
	generated SPI Flas	sh binary image for the	target platform at boot time.	SKL-S	Profile 0	
	Selection is limited Controller Profile clicking on "Add pu Profiles".	d to the profiles defined es "up to maximum 16 p rofile" button under "In				
	The 'Record #' ref Controller Profile	ers to profile created un os".	nder the "Integrated Clock			
	Derault boot profil	e for system is profile (J.			
	Double click on va options.	lue column of this para	meter to choose from available			



Table 2-8. Intel [®] FIT - Integrated Clock Controller (Sheet 2 of 13	able 2-8.	. Intel [®] FIT -	Integrated Clock Controller	(Sheet 2 of 13)
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ŧ		Param	eter	Platform	Settings	
	Failsafe Profile This parameter s failure detection profile if "Integr Policies - Profi parameter is set profile 0 will be s The 'Record #' rr Controller Profi Default Failsafe I	specifies the profile ind or CMOS clear the Intr ated Clock Controlle le Changeable " is se to False, User can not selected as a fail safe t efers to profile created iles".	SKL-Y SKL-U SKL-H SKL-S	Profile 0 Profile 0 Profile 0 Profile 0		
	Double click on voortions.	value column of this pa	rameter to choose from available			
options. Profile Changeable Possible configuration: True/False. This parameter controls if BIOS or 3rd party application can select boot profile or not. When set to true, it allows user to change boot profile via BIOS or 3rd party application. When set to false, Runtime change to boot profile is not allowed and boot profile selected by "Integrated Clock Controller Integrated Clock Controller Policies - Boot Profile " parameter will be used to boot platform. Double click on value column of this parameter to choose from available options. k on Integrated Clock Controller in the left tabs menu> Profiles are expansion.				SKL-Y SKL-U SKL-H SKL-S	true true true true	
▼ Pr	ofiles				3	
▼ P	rofile 2					
	Parameter	Value	Hel	p Text		
Profile	Name	Profile 0	Editable text string.	in he loaded to onching	har ICC profile pattings	
Pronie	rohie Type Standard Specifies the prohie. Intel (R) ME image has to be loaded to enable other ICC prohie settings.					



Table 2-8. Intel[®] FIT - Integrated Clock Controller (Sheet 3 of 13)

#	Parameter	Platform	Settings
	Integrated Clock Controller - Profiles - Profile 0	SKL-Y	Standard
0		SKL-U	Standard
4	For SKL-LP, Intel® FIT provides 2 pre- defined ICC profiles to choose	SKL-H	Standard
	irom.	SKL-S	Standard
	•Standard: This profile provides default settings for standard		
	internal and external are driven from USB3PCIE clock. Default clock		
	frequency is 100 MHz with 0.5%DownSpread. BCLK clock source should be		
	turned off in this case to save power.		
	•Adaptive: This profile provides Wimax/3G friendly configuration. This		
	adaptive clocking adjustment to reduce EML interference		
	addprive clocking adjustment to reduce Livit interference.		
	Note: Intel® ME image has to be loaded to enable other ICC profile		
	Settings.		
	For SKL-H, Intel® FIT provides 4 pre-defined ICC profiles to choose from.		
	· · · · · · · · · · · · · · · · · · ·		
	•Standard: Same as SKL-LP		
	•Adaptive: Same as SKL-LP		
	•Overclocking: This profile provides overclocking friendly configuration.		
	Both Clock sources BCLK and USB3PCIE are turned on in this case. clock		
	0.5% DownSpread, BCLK overclocking can be supported using BCLK clock		
	source.		
	•Overclocking Plus: This profile provides overclocking > 100MHZ for		
	BCLK overclocking.		
	Note: User can select pre-defined profiles via "Integrated Clock Controller Profiles - Profile Type " parameter		
	User can add up to maximum 16 profiles.To add new profile, please use		
	"Integrated Clock Controller Profiles - + Add Profile Button"		
	Profile Name	SKL-Y	Profile 0
		SKL-U	Profile 0
	This parameter allows user to customize profile name for easy	SKL-H	Profile 0
	identification. By default it uses pre-defined profile name like Profile 0.	SKL-S	Profile 0
	Profile Type	SKL-Y	Standard
		SKL-U	Standard
	Available ICC profiles for SKL-LP are Standard and Adaptive.	SKL-H	Standard
		SKL-S	Standard
	Available ICC profiles for SKL-H are Standard, Adaptive, OverClocking,		
	This parameter indicates which pre- defined profile selected for each		
	profile#.		
	Double click on value column of this parameter to choose from available options.		
	+ Add Profile Button		
5	This button is used to add new ICC profile. User can add up to maximum		
	16 profiles. New profile will be added under "Integrated Clock		
1			



Table 2-8. Intel[®] FIT - Integrated Clock Controller (Sheet 4 of 13)

▼ B	ded by default:	4					
	Parameter	Value	Help	Text			
BCLK (Clock Frequency	This parameter is not configura	Select the nominal frequency for the selected c	lock. Range is limited base	ed on the Clock		
BCLK S	Spread setting	This parameter is not configura	Select the percentage of Spread setting for the	selected clock. Range is l	limited based on		
¥		Paramete	er	Platform	Settings		
9	Integrated Cloc BclkClockConfig	k Controller - Profiles guration					
	BCLK Clock Free frequency for the Definition record Standard Settin Adaptive Settin	quency - This parameter selected clock. Range is and HW SKU. g Profile Type - Option g Profile Type - Option	allows user to select the nominal limited based on the Clock Range is grayed out. is able to be edited.				
BCLK Spread Setting - This parameter allows user to select the percentage of Spread setting for the selected clock. Range is limited based on the Clock Range Definition record and HW SKU. BCLK Clock Frequency Standard Setting Profile Type - Option is grayed out. Adaptive Setting Profile Type - Option is able to be edited							
oand	ded by default: ClockRangeDefinitionRed	cord 5					
	Parameter	Value	Help	Text			
BCLK	PLL Clock Source Maxi	This parameter is not configura	Specifies the maximum frequency that can be	applied to BCLK clock sou	rce. Value is limi		
BCLK	PLL Clock Source Mini	This parameter is not configura	. Specifies the minimum frequency that can be	applied to BCLK clock sour	rce.Value is limite		
BLCK SSC Channes Allowed This narameter is not configure Specifies if the spread mode and percentage is allowed to be modified at runtime					runtime.		
BLCK	SSC Halt Allowed	This parameter is not configura	if TRUE , the spread generator can be enabled	and disabled at runtime.			
BLCK BLCK	SSC Percentage	This parameter is not configura	. Specifies the maximum precentage of spread a	adjustment that can be app	lied to the clock		
BLCK BLCK BLCK							
BLCK BLCK BLCK		Paramete	ər	Platform	Settings		
BLCK BLCK BLCK	Integrated Cloc ClockRangeDef	Paramete k Controller - Profiles initionRecord	er - Profile	Platform	Settings		



Table 2-8. Intel[®] FIT - Integrated Clock Controller (Sheet 5 of 13)

#	Parameter			Platform	Settings
	BCLK PLL Clock	Source Minimum Freq			
	source. Value is	limited by divider/frequen	cy limits determined by HW SKU.		
	Standard Settin	ng Profile Type - Option	is grayed out.		
	Adaptive Settin	ng Profile Type - Option			
	BCLK SSC Chan spread mode and	ges Allowed - This parar d percentage is allowed to	neter allows user to specify if the be modified at runtime or not. if		
	set to "True': R	untime modification is allo	owed.		
	Standard Settin	ng Profile Type - Option	is grayed out.		
	Adaptive Settin	ng Profile Type - Option	is able to be edited.		
	spread generator	r can be disabled at runtir	me or not.if set to "True" , the		
	spread generato	r can be enabled and disa	bled at runtime.		
	Standard Settin	ng Profile Type - Option	is grayed out.		
	Adaptive Settin	ng Profile Type - Option	is able to be edited.		
	percentage of sp	entage - This parameter pread adjustment that can	be applied to the clock. Value is		
	specified in 1/10	Oth of percent(50=0.5%)			
	Standard Settin	ng Profile Type - Option	is grayed out.		
	Adaptive Settin	ng Profile Type - Option	is able to be edited.		fi i -
expand	ed by default:	CK Controller in the left	tabs menu> Profiles >Profile>		onfiguration is
	Parameter	Value	Help	Text	
ITPXDP		Enabled	Enable/Disable the CLKOUT_ITPXDP differentiate	al output buffer.	
SRC0		Enabled	Enable/Disable the CLKOUT_SRC0 differential	output buffer.	
SRC1		Enabled	Enable/Disable the CLKOUT_SRC1 differential	output buffer.	
SRC2		Enabled	Enable/Disable the CLKOUT_SRC2 differential	output buffer.	
SRC3		Enabled	Enable/Disable the CLKOUT_SRC3 differential	output buffer.	
SRC4		Enabled	Enable/Disable the CLKOUT_SRC4 differential	output buffer.	
SRC5		Enabled	Enable/Disable the CLKOUT_SRC5 differential	output buffer.	
LPC0	Enabled Enable/Disable the CLKOUT_LPC0 single ended output buffer.				
LPC1		Enabled	Enable/Disable the CLKOUT_LPC1 single end	ed output buffer.	
#		Paramete	er	Platform	Settings
6	Integrated Cloc Configuration	ck Controller - Profiles	- Profile Clock Output		



#	Parameter	Platform	Settings
	ITPXDP,SRC[0:5]	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	These parameters come under the Power Management section and they	SKL-H	Enabled
	control Enabling /Disabling of specific Output Clocks at boot time.	SKL-S	Enabled
	I hese settings should match with platform		
	nardware design.		
	For CDD, recommend keeping defaults for		
	bring up with Intol® ME EW		
	These parameters are specifically used to Enable/Disable the respective		
	CLKOUT_XXX differential output buffers		
-	SDC0[4:15]	SKLV	Epoblod
	Values: Enabled /Disabled	SKL-1	Enabled
	These parameters come under the Power Management section and they	SKL-H	Enabled
	control Enabling /Disabling of specific Output Clocks at boot time.	SKL-S	Enabled
	These settings should match with platform	SILE S	Enabled
	hardware design.		
	For CRB, recommend keeping defaults for		
	bring up with Intel® ME FW.		
	These parameters are specifically used to Enable/Disable the respective		
		CKL V	Frahlad
	SRC I Values: Enabled / Disabled	SKL-T	Enabled
	Enables or Disables the CLKOUT SPC1 differential output buffer	SKL-U	Enabled
		SKL-II	Enabled
	SPC2	SKL-V	Enabled
	Values: Enabled/Disabled	SKL	Enabled
	Enables or Disables the CLKOUT_SRC2 differential output buffer	SKI-H	Enabled
		SKL-S	Enabled
	SPC3	SKI-V	Enabled
	Values: Enabled/Disabled	SKI-U	Enabled
	Enables or Disables the CLKOUT_SRC3 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	SRC4	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	Enables or Disables the CLKOUT_SRC4 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	SRC5	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	Enables or Disables the CLKOUT_SRC5 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	SRC6	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	Enables or Disables the CLKOUT_SRC6 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	SRC7	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	Enables or Disables the CLKOUT_SRC7 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled

Table 2-8. Intel[®] FIT - Integrated Clock Controller (Sheet 6 of 13)



Table 2-8. Intel[®] FIT - Integrated Clock Controller (Sheet 7 of 13)

#	Parameter	Platform	Settings
	SRC8	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	Enables or Disables the CLKOUT_SRC8 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	SRC9	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	Enables or Disables the CLKOUT_SRC9 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	SRC10	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	Enables or Disables the CLKOUT_SRC10 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	SRC11	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	Enables or Disables the CLKOUT_SRC11 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	SRC12	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	Enables or Disables the CLKOUT_SRC12 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	SRC13	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	Enables or Disables the CLKOUT_SRC13 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	SRC14	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	Enables or Disables the CLKOUT_SRC14 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	SRC15	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	Enables or Disables the CLKOUT_SRC15 differential output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	LPC0[1:0]	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	These parameters are used to control Enabling/Disabling of CLKRUN	SKL-H	Enabled
	support for CLKOUT_LPC clocks.	SKL-S	Enabled
	For CRB, recommend keeping defaults for		
	bring up with Intel® ME FW		
	LPC1	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	Enables or Disables the CLKOUT_LPC1 single ended output buffer.	SKL-H	Enabled
		SKL-S	Enabled
	CPUPCIBCLK	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	Enables or Disables the CPUPCIBCLK output buffer.	SKL-H	Enabled
		SKL-S	Enabled



Table 2-8. Intel[®] FIT - Integrated Clock Controller (Sheet 8 of 13)

Click on Integrated Clock Controller in the left tabs menu> Profiles >Profile> Power Management Configuration is expanded by default:

Parameter	Value	Help Text
SRC0 CLKREQ# Mapping	GPP_B5	Assign the CLKREQ# signal associated with CLKO
SRC1 CLKREQ# Mapping	GPP_B6	Assign the CLKREQ# signal associated with CLKO
SRC2 CLKREQ# Mapping	GPP_B7	Assign the CLKREQ# signal associated with CLKO
SRC3 CLKREQ# Mapping	GPP_B8	Assign the CLKREQ# signal associated with CLKO
SRC4 CLKREQ# Mapping	GPP_B9	Assign the CLKREQ# signal associated with CLKO
SRC5 CLKREQ# Mapping	GPP_B10	Assign the CLKREQ# signal associated with CLKO
CLKREQ SRC0 Enable	Enabled	Enable/Disable the dynamic clock request control
CLKREQ SRC1 Enable	Enabled	Enable/Disable the dynamic clock request control
CLKREQ SRC2 Enable	Enabled	Enable/Disable the dynamic clock request control
CLKREQ SRC3 Enable	Enabled	Enable/Disable the dynamic clock request control
CLKREQ SRC4 Enable	Enabled	Enable/Disable the dynamic clock request control
CLKREQ SRC5 Enable	Enabled	Enable/Disable the dynamic clock request control
CLKRUN LPC0 Enable	Enabled	Enable/Disable the CLKRUN protocol on LPC0 outp
CLKRUN LPC1 Enable	Enabled	Enable/Disable the CLKRUN protocol on LPC1 outp
Clock Gating of Core 24Mhz Cry	Enabled	Enable/Disable dynamic clock gating of Core 24M
Clock Gating of CLKOUT_ITPxD	Enabled	Enable/Disable dynamic control of CLKOUT_ITPx
Clock Gating of CLKOUT_CPUBC	Enabled	Enable/Disable dynamic control of CLKOUT_CPUB
Clock Gating of CLKOUT_CPUNS	Enabled	Enable/Disable dynamic control of CLKOUT_CPUN
Clock Gating of CLKOUT_CPUNS	Enabled	Enable/Disable dynamic control of CLKOUT_CPUN
Clock Gating of icc_rosc_fast_cl	Enabled	Enable/Disable dynamic clock gate on icc_rosc_fa
Clock Gating of icc_rosc_side_cl	Enabled	Enable/Disable dynamic clock gate on icc_rosc_si
USB3Gen2PCIe PLL OFF Wait	8us	Set G2PLLOFFWAIT timer value. Once timer expr
USB3Gen2PCIe PLL PG Wait	8us	Set G2PLLPGWAIT timer value. Once timer expri
Run-time S0 SUS PG Wait	8us	Set SUSPGWAIT timer value. Once timer exprire
Crystal Oscillator Fast Restart	01b	Configure Crystal Oscillator Fast Restart Mode. In
BCLK PLL Shutdown Wait Interval	8us	Enable Dynamic power management of BCLK PLL
24Mhz Crystal Shutdown Wait L.	8us	Enable Dynamic power management of Crystal, I



Table 2-8. Intel[®] FIT - Integrated Clock Controller (Sheet 9 of 13)

Integrated Clock Controller - Profile PwrMaagementConfiguration Skill CP Recipe of Clock Recover Amplitude Possible configuration Skill CPP_B5 Possible configuration Skill CPP_B5 Possible configuration Skill CPP_B5 This parameter controls association of dynamic CLKREQ control with SRC (PCIe) clocks. Skill CPP_B5 SRC15:61 CLKREC# Mapping - Skill - H Only Possible configurations association of dynamic CLKREQ control with SRC (PCIe) clocks. Skill CPP_B6 SRC2 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC1. Skill CPP_B6 SRC2 CLKREQ# signal associated with CLKOUT_SRC2. Skill CPP_B6 SRC3 CLKREQ# signal associated with CLKOUT_SRC3. Skill GPP_B7 SRC3 CLKREQ# signal associated with CLKOUT_SRC3. Skill GPP_B7 SRC4 CLKREQ# signal associated with CLKOUT_SRC3. Skill GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC3. Skill GPP_B7 SRC4 CLKREQ# signal associated with CLKOUT_SRC4. GPP_B7 Skill GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC5. Skill GPP_B7 SRC5 CLKREQ# signal associate	#	Parameter	Platform	Settings
PwrManagementConfiguration SRC0[5:0] CLKREO# Mapping SKLV GPP_B5 Possible configuration: Select one of the GPIOs from the list to map it as a CLKREO# for specific SK2 # 01tput clck. SKL-U GPP_B5 This parameter controls association of dynamic CLKREQ control with SRC (PC) clocks. SKL-U GPP_B5 SRC1[5:6] CLKREO# Mapping - SKL - H Only SKL-W GPP_B6 Possible configuration: Select one of the GPIOs from the list to map it as a CLKREO# for specific SRC# Output put clock. SKL-W GPP_B6 SRC1[CLKREO# Mapping SKL-W GPP_B6 SKL-W GPP_B6 Assign the CLKREO# Mapping SKL-W GPP_B6 SKL-H GPP_B6 SRC2 CLKREO# Mapping SKL-W GPP_B7 SKL-H GPP_B7 Assign the CLKREO# signal associated with CLKOUT_SRC2. SKL-H GPP_B7 SKL-H GPP_B7 Assign the CLKREO# signal associated with CLKOUT_SRC3. SKL-Y GPP_B7 GPP_B7 Assign the CLKREO# signal associated with CLKOUT_SRC4. SKL-Y GPP_B7 GPP_B7 Assign the CLKREO# signal associated with CLKOUT_SRC5. SKL-W GPP_B7 GPP_B7 Assign the CLKREO# signal associated with CLKO		Integrated Clock Controller - Profiles - Profile		
SRC0[5:0] CLKREC# Mapping SKL GPP_B5 Possible configuration: Select one of the GPIOs from the list to map it as a CLKREO# for specific SRC# Output clock. SKL GPP_B5 This parameter controls association of dynamic CLKREO control with SRC (PC1e) clocks. GPP_B5 SKL+ GPP_B5 SRC[15:6] CLKREC# Mapping - SKL - H Only SKL-Y GPP_B6 GPP_B6 Possible configuration: Select one of dynamic CLKREQ control with SRC (PC1e) clocks. SKL-Y GPP_B6 SRC[15:6] CLKREC# Mapping SKL + H Only SKL-Y GPP_B6 Assign the CLKREC# Mapping SKL + GPP_B6 SKL-Y GPP_B6 SRC2 CLKREC# Mapping SKL + GPP_B7 SKL + GPP_B7 Assign the CLKREC# fignal associated with CLKOUT_SRC1. SKL + GPP_B7 GPP_B7 SRC3 CLKREC# Mapping SKL + GPP_B7 GPP_B8 Assign the CLKREC# signal associated with CLKOUT_SRC3. SKL + GPP_B7 SRC4 CLKREC# Mapping SKL + GPP_B9 Assign the CLKREC# signal associated with CLKOUT_SRC4. SKL + GPP_B9 SRC5 CLKREC# Mapping SKL + GPP_B10 Assign the CLKREC# signal associated with CLKOUT_SRC5. SKL + GPP_B10 SRC5 CLKREC# Mapping SKL + GPP_B10 Assign the CLKREC# signal associated with CLKOUT_SRC6. SKL + GPP_B10 SRC5 CLKREC# Mapping SKL + GPP_B10 <td< td=""><td></td><td>PwrManagementConfiguration</td><td></td><td></td></td<>		PwrManagementConfiguration		
SRC0[5:0] CLKREO# Mapping SKL-Y GPP_B5 Possible configuration: Select one of the GPI0s from the list to map it as a CLKREO# for specific SRC# Output clock. SKL-H GPP_B5 This parameter controls association of dynamic CLKREO control with SRC (PCI6) clocks. GPP_B5 GPP_B5 SRC15:6] CLKREO# Mapping - SKL - H Only SKL-Y GPP_B6 Possible configuration: Select one of the GPI0s from the list to map it as a CLKREO# for specific SRC# Output put clock. SKL-Y GPP_B6 SRC1 CLKREO# Mapping SKL-Y GPP_B6 Assign the CLKREO# Mapping SKL-Y GPP_B6 SRC2 CLKREO# Mapping SKL-Y GPP_B6 SRC2 CLKREO# Mapping SKL-Y GPP_B6 SRC3 CLKREO# Mapping SKL-Y GPP_B7 Assign the CLKREO# Mapping SKL-Y GPP_B8 Assign the CLKREO# Mapping SKL-Y GPP_B8 SRC3 CLKREO# Mapping SKL-Y GPP_B8 Assign the CLKREO# Mapping SKL-Y GPP_B8 SRC4 CLKREO# Mapping SKL-Y GPP_B8 SRC4 CLKREO# Mapping SKL-Y GPP_B9 SRC5 CLKREO# Mapping SKL-Y GPP_B9 Assign the CLKREO# Mapping SKL-Y GPP_B10 SRC4 CLKREO# Mapping SKL-Y GPP_B10 SRC4 CLKREO# Mapping SKL-Y				
SRC103:01 CLKREQ# for specific SRC# Output clock. GPP_B5 This parameter controls associated of ynamic CLKREQ control with SRC (PC16) clocks. GPP_B5 SRC15:61 CLKREQ# Mapping - SKL - H Only SKL-W GPP_B6 Possible configuration: Select one of the GPI0s from the list to map it as a CLKREQ# for specific SRC# Output put clock. SKL-W GPP_B6 This parameter controls associated with CLKOUT_SRC1. SKL-W GPP_B6 SRC2 CLKREQ# Mapping SKL-W GPP_B6 Assign the CLKREQ# signal associated with CLKOUT_SRC1. SKL-W GPP_B7 SRC3 CLKREQ# Mapping SKL-W GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC2. SKL-W GPP_B7 SRC3 CLKREQ# Mapping SKL-W GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-W GPP_B8 SRC4 CLKREQ# Mapping SKL-W GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-W GPP_B8 SRC5 CLKREQ# Mapping SKL-W GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-W GPP_B9 SRC5 CLKREQ# Mapping SKL-W GPP_B10 SRC5 CLKREQ# Mapping SKL-W GPP_B10 <				
CLKREC# for specific SRC# Output clock. SRC: U GP_B5 This parameter controls association of dynamic CLKREQ control with SRC (PCIe) clocks. GP_B5 GP_B5 SRC[15:6] CLKREQ# Mapping - SKL - H Only Possible configuration: Select one of the GPIOs from the list to map it as a CLKREQ# for specific SRC# Output clock. GP_B6 SRC1CCLKREQ# Mapping SKL - H Only Possible configuration: Select one of the GPIOs from the list to map it as a CLKREQ# Mapping SKL - U GPP_B6 SRC1CCLKREQ# Mapping SKL - U GPP_B6 Assign the CLKREQ# Mapping SKL - U GPP_B6 SRC2 CLKREQ# Mapping SKL - U GPP_B7 Assign the CLKREQ# dispal associated with CLKOUT_SRC1. SKL - U GPP_B7 SRC3 CLKREQ# Mapping SKL - U GPP_B8 Assign the CLKREQ# dispal associated with CLKOUT_SRC3. SKL - U GPP_B8 SRC4 CLKREQ# Mapping SKL - U GPP_B9 SRC5 CLKREQ# Mapping SKL - U GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL - U GPP_B9 SRC5 CLKREQ# Mapping SKL - U GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL - U GPP_B10 SRC5 CLKREQ# Mapping SKL - U GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL - U NA SRC5 CLKREQ#		SRCU[5:0] CLKREQ# Mapping	SKL-Y	GPP_B5
This parameter controls association of dynamic CLKREQ control with SRC (PCIe) clocks. SKL-S GPP_B5 SRC115-61 CLKREO# Mapping - SKL - H Only Possible configuration. Select one of the GPIOs from the list to map it as a CLKREO# for specific SRC# Output put clock. This parameter controls association of dynamic CLKREQ control with SRC (PCIe) clocks. GPP_B6 SKL-T CLKREO# Mapping Assign the CLKREO# signal associated with CLKOUT_SRC1. SKL-Y GPP_B6 SKC2 CLKREO# Mapping Assign the CLKREO# signal associated with CLKOUT_SRC2. SKL-Y GPP_B7 SRC3 CLKREO# Mapping Assign the CLKREO# signal associated with CLKOUT_SRC3. SKL-Y GPP_B8 SRC4 CLKREO# Mapping Assign the CLKREO# signal associated with CLKOUT_SRC3. SKL-Y GPP_B8 SRC4 CLKREO# Mapping Assign the CLKREO# signal associated with CLKOUT_SRC4. SKL-Y GPP_B9 SRC4 CLKREO# Mapping Assign the CLKREO# signal associated with CLKOUT_SRC4. SKL-Y GPP_B9 SRC5 CLKREO# Mapping Assign the CLKREO# signal associated with CLKOUT_SRC5. SKL-Y GPP_B10 SRC6 CLKREO# Mapping Assign the CLKREO# signal associated with CLKOUT_SRC6. SKL-Y NA SRC6 CLKREO# signal associated with CLKOUT_SRC6. SKL-Y NA SRC6 CLKREO# signal associated with CLKOUT_SRC6. SKL-Y NA SRC7 CLKREO# Mapping Assign the CLKREO# signal associated with CLKOUT_SRC6.		CLKREQ# for specific SRC# Output clock.	SKL-U	GPP_B5
(PCIe) clocks. Number of the CPLOS from the list to map it as a CLKREO# Mapping - SKL - H Only Possible configuration: Select one of the CPLOS from the list to map it as a CLKREO# for specific SRC# Output put clock. SKL This parameter controls associated with CLKOUT_SRC1. SKL-U SRC1 CLKREO# Mapping SKL-Y Assign the CLKREO# signal associated with CLKOUT_SRC1. SKL-U SRC2 CLKREO# Mapping SKL-Y Assign the CLKREO# signal associated with CLKOUT_SRC2. SKL-U SRC3 CLKREO# Mapping SKL-Y Assign the CLKREO# signal associated with CLKOUT_SRC2. SKL-H SRC3 CLKREO# Mapping SKL-Y Assign the CLKREO# signal associated with CLKOUT_SRC3. SKL-H SRC4 CLKREO# Mapping SKL-Y Assign the CLKREO# signal associated with CLKOUT_SRC4. SKL-U SRC5 CLKREO# Mapping SKL-S Assign the CLKREO# signal associated with CLKOUT_SRC5. SKL-U SRC5 CLKREO# Mapping SKL-Y Assign the CLKREO# signal associated with CLKOUT_SRC5. SKL-Y SRC6 CLKREO# signal associated with CLKOUT_SRC6. SKL-Y SRC6 CLKREO# signal associated with CLKOUT_SRC7. SKL-U SRC6 CLKREO# signal associated with CLKOUT_SRC7. SKL-U		This parameter controls association of dynamic CLKREQ control with SRC	SKL-S	GPP B5
SRC15:6] CLKREO# Mapping - SKL - H Only SRC15:6] CLKREO# Mapping SRC10:6 SRC 0Upting Ut Clck. This parameter controls association of dynamic CLKREQ control with SRC (PC) clocks. SRC1 ULKREO# Mapping SKL U GPP_B6 Assign the CLKREO# signal associated with CLKOUT_SRC1. SKL U GPP_B6 SKL-Y GPP_B7 Assign the CLKREO# Mapping SKL W GPP_B7 SKL-Y GPP_B7 Assign the CLKREO# signal associated with CLKOUT_SRC2. SKL-H GPP_B7 SRC3 CLKREO# Mapping SKL-Y GPP_B7 Assign the CLKREO# signal associated with CLKOUT_SRC3. SKL-U GPP_B8 SRC3 CLKREO# Mapping SKL-S GPP_B9 Assign the CLKREO# signal associated with CLKOUT_SRC3. SKL-U GPP_B9 SRC4 CLKREO# signal associated with CLKOUT_SRC4. SKL-U GPP_B9 Assign the CLKREO# signal associated with CLKOUT_SRC5. SKL-Y GPP_B9 SRC5 CLKREO# Mapping SKL-Y GPP_B10 Assign the CLKREO# signal associated with CLKOUT_SRC5. SKL-Y GPP_B10 SRC6 CLKREO# signal associated with CLKOUT_SRC5. SKL-Y MA SRC6 CLKREO# Mapping SKL-Y NA SKL-S Assign the CLKREO#		(PCIe) clocks.		
SRC115-61 CLKREQ# Mapping - SkL - H Only SkL - H Only Possible configuration: Select one of the GPDs from the list to map it as a CLKREQ# for specific SRC# Output put clock. SkL SRC1 CLKREQ# Mapping SkL.Y GPP_B6 Assign the CLKREQ# signal associated with CLKOUT_SRC1. SkL.H GPP_B6 SRC2 CLKREQ# Mapping SkL.Y GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC2. SkL.H GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SkL.Y GPP_B7 SRC3 CLKREQ# Mapping SkL.Y GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SkL.H GPP_B8 SRC4 CLKREQ# signal associated with CLKOUT_SRC3. SkL.H GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SkL.U GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SkL.H GPP_B10 SRC5 CLKREQ# Mapping SkL.Y GPP_B10 SkL.H GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SkL.H GPP_B10 SkL.H GPP_B10 SRC6 CLKREQ# signal associated with CLKOUT_SRC6. SkL.H GPP_H0 SkL.S GPP_H0 SRC7 CLKREQ# signal associated with C				
Prosible Configuration: Select One Of the OFLOS From the list to map it as a CLKREQ# for specific SR0# Output pt clock. SRC This parameter controls associated of dynamic CLKREQ control with SRC (PCIe) clocks. SRL CLKREQ# Mapping SRL-V GPP_B6 Assign the CLKREQ# signal associated with CLKOUT_SRC1. SRL-V GPP_B6 SRC2 CLKREQ# Mapping SRL-Y GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC2. SRL-H GPP_B7 SRC3 CLKREQ# Mapping SRL-Y GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SRL-H GPP_B8 SRC4 CLKREQ# Mapping SRL-Y GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SRL-U GPP_B8 SRC4 CLKREQ# Mapping SRL-Y GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SRL-H GPP_B9 SRC5 CLKREQ# Mapping SRL-Y GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SRL-U GPP_B10 SRC5 CLKREQ# Mapping SRL-Y GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC6. SRL-U NA SRC7 CLKREQ# Mapping SRL-Y NA Assign the CLKREQ# signal associated wit		SRC[15:6] CLKREQ# Mapping - SKL - H Only		
This parameter controls association of dynamic CLKREQ control with SRC (PCIe) clocks. SKL GPP_B6 SRC1 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC1. SKL-H GPP_B6 SRC2 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC2. SKL-H GPP_B7 SRC3 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-U GPP_B7 SRC3 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-U GPP_B8 SRC4 CLKREQ# signal associated with CLKOUT_SRC3. SKL-U GPP_B9 SRC4 CLKREQ# signal associated with CLKOUT_SRC4. SKL-U GPP_B9 SRC5 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B9 SRC5 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B10 SRC6 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-U NA SRC6 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-U NA SRC7 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-U NA SRC6 CLKREQ# signal associated with CLKOUT_SRC6. SKL-U NA SKL-S GPP_H1 SRC9 CLKREQ# signal associated with CLKOUT_SRC7. SKL-U </td <td></td> <td>CLKREO# for specific SRC# Output put clock.</td> <td></td> <td></td>		CLKREO# for specific SRC# Output put clock.		
(PC1e) clocks. SRC1 CLKREQ# Mapping SKL-Y GPP_B6 Assign the CLKREQ# signal associated with CLKOUT_SRC1. SKL-U GPP_B6 SRC2 CLKREO# Mapping SKL-S GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC2. SKL-U GPP_B7 SRC3 CLKREO# Mapping SKL-H GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC2. SKL-H GPP_B7 SRC3 CLKREO# Mapping SKL-H GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-H GPP_B8 SRC4 CLKREQ# signal associated with CLKOUT_SRC4. SKL-H GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-H GPP_B9 SRC5 CLKREQ# Mapping SKL-H GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B10 SRC6 CLKREQ# signal associated with CLKOUT_SRC6. SKL-V NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-V NA SRC6 CLKREQ# signal associated with CLKOUT_SRC6. SKL-V NA SRC6 CLKREQ# signal associated with CLKOUT_SRC7. SKL-V NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-V		This parameter controls association of dynamic CLKREQ control with SRC		
SRC1 CLKREO# Mapping SKL-V GPP_B6 Assign the CLKREQ# signal associated with CLKOUT_SRC1. SKL-W GPP_B6 SRC2 CLKREO# Mapping SKL-W GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC2. SKL-W GPP_B7 SRC3 CLKREO# Mapping SKL-W GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-W GPP_B8 SRC4 CLKREQ# signal associated with CLKOUT_SRC3. SKL-W GPP_B8 SRC4 CLKREQ# signal associated with CLKOUT_SRC3. SKL-W GPP_B8 SRC4 CLKREQ# signal associated with CLKOUT_SRC3. SKL-W GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-W GPP_B9 SRC5 CLKREO# Mapping SKL-W GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-W GPP_B10 SRC6 CLKREO# Mapping SKL-W GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-W GPP_B10 SRC6 CLKREO# Mapping SKL-W NA SKL-W Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-W NA SRC7 CLKREO# Mapping SKL-W NA SKL-S GPP_H0		(PCIe) clocks.		
Assign the CLKREQ# signal associated with CLKOUT_SRC1. SKL-U GPP_B6 SRC2 CLKREQ# Mapping SKL-S GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC2. SKL-U GPP_B7 SRC3 CLKREQ# Mapping SKL-V GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-V GPP_B8 SRC4 CLKREQ# dignal associated with CLKOUT_SRC3. SKL-U GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-V GPP_B9 SRC4 CLKREQ# dignal associated with CLKOUT_SRC4. SKL-V GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-V GPP_B9 SRC5 CLKREQ# mapping SKL-Y GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B10 SRC6 CLKREQ# mapping SKL-Y NA SKL-S Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SKL-S SRC7 CLKREQ# mapping SKL-Y NA SKL-S GPP_H0 SRC6 CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SKL-S GPP_H0 SRC7 CLKREQ# mapping SKL-Y NA SKL-S GPP_H1		SRC1 CLKREQ# Mapping	SKL-Y	GPP_B6
SRC2 CLKREQ# Mapping SRL-H GPP_B6 SRC2 CLKREQ# signal associated with CLKOUT_SRC2. SKL-U GPP_B7 Assign the CLKREQ# Mapping SKL-U GPP_B7 SRC3 CLKREQ# Mapping SKL-Y GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-U GPP_B8 SRC4 CLKREQ# Mapping SKL-Y GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-H GPP_B9 SRC4 CLKREQ# Mapping SKL-Y GPP_B9 Assign the CLKREQ# mapping SKL-Y GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-U GPP_B9 SRC5 CLKREQ# Mapping SKL-Y GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-Y GPP_B10 SRC6 CLKREQ# Mapping SKL-Y NA SKL-S Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SRC7 CLKREQ# Mapping SKL-Y NA SKL-S Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-Y NA SRC7 CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA SRC9 CLKREQ# Mapping SKL-Y		Assign the CLKREQ# signal associated with CLKOUT_SRC1.	SKL-U	GPP_B6
SRC2 CLKREO# Mapping SRL-Y GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC2. SKL-U GPP_B7 SRC3 CLKREQ# Mapping SKL-H GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-V GPP_B8 SRC4 CLKREQ# Mapping SKL-V GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-U GPP_B9 SRC4 CLKREQ# mapping SKL-Y GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-Y GPP_B9 SRC5 CLKREQ# Mapping SKL-Y GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-Y GPP_B9 SRC5 CLKREQ# Mapping SKL-Y GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SRC5 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SRC5 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-Y NA SRC5 CLKREQ# Mapping SKL-Y NA SKL-S GPP_H1 SRC6 CLKREQ# Mapping SKL-Y			SKL-H	GPP_B6
SRC2 CLKREQ# Mapping SKL-Y GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC2. SKL-U GPP_B7 SRC3 CLKREQ# Mapping SKL-Y GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-V GPP_B8 SRC4 CLKREQ# Mapping SKL-Y GPP_B8 Assign the CLKREQ# mapping SKL-Y GPP_B8 SRC4 CLKREQ# Mapping SKL-Y GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-Y GPP_B9 SRC5 CLKREQ# Mapping SKL-Y GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B10 SRC4 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B10 SRC4 CLKREQ# Mapping SKL-Y NA SKL-S Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-U NA SKL-S SRC5 CLKREQ# Mapping SKL-Y NA SKL-S GPP_H0 SRC5 CLKREQ# Mapping SKL-Y NA SKL-S GPP_H0 SRC6 CLKREQ# Mapping SKL-Y NA SKL-S GPP_H1			SKL-S	GPP_B6
Assign the CLKREO# signal associated with CLKOUT_SRC2. SRL-U GPP_B7 SRC3 CLKREO# Mapping SKL-V GPP_B7 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-U GPP_B8 SRC4 CLKREQ# Mapping SKL-V GPP_B8 SRC4 CLKREQ# Mapping SKL-V GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-U GPP_B9 SRC5 CLKREQ# Mapping SKL-V GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B9 SRC6 CLKREQ# Mapping SKL-V GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B10 SRC6 CLKREQ# Mapping SKL-V NA SKL-S Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-U NA SRC7 CLKREQ# Mapping SKL-V NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-U NA SRC8 CLKREQ# Mapping SKL-V NA SKL-S GPP_H1 SRC9 CLKREQ# Mapping SKL-V NA SKL-S GPP_H1 SRC9 CLKREQ# Mapping SKL-V NA SKL-S GPP_H2 <t< td=""><td></td><td>SKU2 ULKREQ# Mapping</td><td>SKL-Y</td><td>GPP_B7</td></t<>		SKU2 ULKREQ# Mapping	SKL-Y	GPP_B7
SRL-R GPP_B7 SRC3 CLKREQ# Mapping SKL-Y GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-U GPP_B8 SRC4 CLKREQ# Mapping SKL-S GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-U GPP_B9 SRC5 CLKREQ# Mapping SKL-Y GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-V GPP_B9 SRC5 CLKREQ# Mapping SKL-Y GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-V GPP_B10 SRC5 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-V NA SRC5 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-V NA SRC7 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-U NA SRC8 CLKREQ# signal associated with CLKOUT_SRC8. SKL-V NA SRC9 CLKREQ# signal associated with CLKOUT_SRC8. SKL-V NA SRC9 CLKREQ# signal associated with CLKOUT_SRC9. SKL-V NA <td< td=""><td></td><td>Assign the CLKREQ# signal associated with CLKOUT_SRC2.</td><td>SKL-U</td><td>GPP_B/</td></td<>		Assign the CLKREQ# signal associated with CLKOUT_SRC2.	SKL-U	GPP_B/
SRC3 CLKREC# Mapping SKL-Y GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-Y GPP_B8 SRC4 CLKREQ# Mapping SKL-S GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-H GPP_B9 SRC5 CLKREQ# Mapping SKL-H GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-H GPP_B9 SRC5 CLKREQ# Mapping SKL-Y GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-H GPP_B10 SRC5 CLKREC# Mapping SKL-Y GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-Y NA SRC6 CLKREC# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SRC7 CLKREO# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-U NA SRC7 CLKREO# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-U NA SRC8 CLKREO# Mapping SKL-U NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA SRC9 CLKREO# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-U NA			SKL-H	GPP_D7
Assign the CLKREQ# signal associated with CLKOUT_SRC3. SKL-U GPP_B8 SRC4 CLKREQ# Mapping SKL-W GPP_B8 SRC4 CLKREQ# Mapping SKL-W GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-W GPP_B9 SRC5 CLKREQ# Mapping SKL-W GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-W GPP_B10 SRC5 CLKREQ# Mapping SKL-W GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-W GPP_B10 SRC6 CLKREQ# Mapping SKL-W SKL-W Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-W NA SRC6 CLKREQ# Mapping SKL-W NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-W NA SRC7 CLKREQ# Mapping SKL-W NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-W NA SRC8 CLKREQ# Mapping SKL-W NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-W NA SRC9 CLKREQ# signal associated with CLKOUT_SRC9. SKL-W NA SKL-Y NA SKL-Y NA		SPC3 CLKPEO# Mapping	SKL-V	
Nongin the CalkREQ# Mapping SRC4 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-W GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-U GPP_B9 SRC5 SRC4 GPP_B9 SKL-H GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B10 SRC5 SKLEQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B10 SRC6 SKLEQ# Mapping SKL-Y GPP_B10 SRC6 SKLEQ# signal associated with CLKOUT_SRC5. SKL-W GPP_B10 SRC6 SKLEQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-W NA SRC7 SKLEQ# signal associated with CLKOUT_SRC7. SKL-V NA SRC7 SKLREQ# mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-V NA SRC9 SKLREQ# mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA SRC9 SKLREQ# mapping SKL-Y NA SKLS GPP_H2		Assign the CLKREO# signal associated with CLKOUT_SRC3	SKI-U	GPP_B8
SRC4 CLKREO# Mapping SKL-S GPP_B8 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-Y GPP_B9 SRC5 CLKREO# Mapping SKL-S GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-Y GPP_B10 SRC5 CLKREQ# Mapping SKL-Y GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-Y GPP_B10 SRC6 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SRC7 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SRC7 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-Y NA SRC8 CLKREO# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-V NA SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-U NA SRC10 CLKREQ# signal associated with CLKOUT_SRC9. SKL-V NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-V NA SKL-B GPP_H3 SK			SKL-H	GPP B8
SRC4 CLKREQ# Mapping SKL-Y GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-U GPP_B9 SRC5 CLKREQ# Mapping SKL-Y GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-Y GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-Y GPP_B10 SRC6 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SRC7 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SRC7 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-U NA SRC8 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SKL-B GPP_H2 SKL-S GPP_H3 SKL-B GPP_H3 SKL-Y NA </td <td></td> <td></td> <td>SKL-S</td> <td>GPP_B8</td>			SKL-S	GPP_B8
Assign the CLKREQ# signal associated with CLKOUT_SRC4. SKL-U GPP_B9 SRC5 CLKREQ# Mapping SKL-S GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-Y GPP_B10 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B10 SRC6 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-V NA SRC6 CLKREQ# dapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-V NA SRC7 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-U NA SRC7 CLKREQ# signal associated with CLKOUT_SRC7. SKL-U NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-V NA SRC9 CLKREQ# mapping SKL-Y NA SKL-Y Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-V NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA <td></td> <td>SRC4 CLKREQ# Mapping</td> <td>SKL-Y</td> <td>GPP_B9</td>		SRC4 CLKREQ# Mapping	SKL-Y	GPP_B9
SRC5 CLKREQ# Mapping SKL-H GPP_B9 Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B10 SRC6 CLKREQ# Mapping SKL-U GPP_B10 SRC6 CLKREQ# Mapping SKL-H GPP_B10 SRC6 CLKREQ# Mapping SKL-V NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-V NA SRC7 CLKREQ# Mapping SKL-V NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-V NA SRC7 CLKREQ# Mapping SKL-V NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-V NA SRC8 CLKREQ# Mapping SKL-V NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-V NA SRC8 CLKREQ# Mapping SKL-V NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-V NA SRC9 CLKREQ# Mapping SKL-V NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-V NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-V NA SKL-S GPP_H3 SKL-S GPP_H4 SKL-S GPP_H4 SKL-S GPP_H4		Assign the CLKREQ# signal associated with CLKOUT_SRC4.	SKL-U	GPP_B9
SRC5CLKREQ# MappingSKL-SGPP_B9Assign the CLKREQ# signal associated with CLKOUT_SRC5.SKL-YGPP_B10SRC6CLKREQ# mappingSKL-HGPP_B10SRC6SKLCGPP_B10SRC6SKL-WNAAssign the CLKREQ# signal associated with CLKOUT_SRC6.SKL-VNASRC7CLKREQ# mappingSKL-YNAAssign the CLKREQ# signal associated with CLKOUT_SRC7.SKL-YNASRC7SKC9GPP_H0SRC8CLKREQ# signal associated with CLKOUT_SRC7.SKL-VNAAssign the CLKREQ# signal associated with CLKOUT_SRC7.SKL-VNASRC8SKREQ# MappingSKL-YNAAssign the CLKREQ# signal associated with CLKOUT_SRC8.SKL-VNASRC9SKREQ# MappingSKL-VNAAssign the CLKREQ# signal associated with CLKOUT_SRC8.SKL-UNASRC9SKREQ# MappingSKL-VNAAssign the CLKREQ# signal associated with CLKOUT_SRC9.SKL-UNASRC10SRC10SKL-HGPP_H2SRC10SRC10SKL-YNAAssign the CLKREQ# signal associated with CLKOUT_SRC10.SKL-YNASKL-SGPP_H3SKL-YNASKL-SGPP_H4SKL-SGPP_H4SKL-SGPP_H4SKL-SGPP_H4SKL-SGPP_H4SKL-SGPP_H4SKL-SGPP_H4SKL-SGPP_H4			SKL-H	GPP_B9
SRC5 CLKREO# Mapping SKL-Y GPP_B10 Assign the CLKREO# signal associated with CLKOUT_SRC5. SKL-U GPP_B10 SRC6 CLKREO# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SRC7 CLKREO# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SRC7 CLKREO# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-Y NA SRC8 CLKREO# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-Y NA SRC8 CLKREO# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA SRC9 CLKREO# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKL-S GPP_H3 SKL-S GPP_H4 SKL-S GPP_H4 SKL-S GPP_H4			SKL-S	GPP_B9
Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-U GPP_B10 SRC6 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-U NA SRC7 CLKREQ# Mapping SKL-H GPP_H0 SRC7 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SRC7 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-Y NA SRC8 CLKREQ# mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SKL-S GPP_H13 SKL-S GPP_H3 SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKL-U NA SKL-S GPP_H4 SKL-S GPP_H4 SKL-S GPP_H4		SRC5 CLKREQ# Mapping	SKL-Y	GPP_B10
SRC4 CLKREQ# Mapping SKL-H GPP_B10 SRC6 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-Y NA SRC7 CLKREQ# Mapping SKL-H GPP_H0 SRC7 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-W NA SRC8 CLKREQ# Mapping SKL-H GPP_H1 SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-H GPP_H1 SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-U NA SRC9 CLKREQ# Mapping SKL-S GPP_H2 SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SRC10 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKL-H GPP_H3 SKL-Y NA SKL-H GPP_H4 SKL-H		Assign the CLKREQ# signal associated with CLKOUT_SRC5.	SKL-U	GPP_B10
SRC6 CLKREQ# Mapping SKL-S GPP_BT0 Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-V NA SRC7 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-W NA SRC8 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-W NA SRC8 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-W NA SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKL-Y NA SKL-S GPP_H3 SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKL-H GPP_H3 SKL-Y NA SKL-H GPP_H4 SKL-Y SKL-Y			SKL-H	GPP_B10
SRC6 CLKREQ# Mapping SRL+Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC6. SKL-W NA SRC7 CLKREQ# Mapping SKL-S GPP_HO SRC7 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-W NA SRC8 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-W NA SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SRC10 CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKL-Y NA SKL-Y NA SKL-Y NA SKL-Y NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-W NA SKL-H <td< td=""><td></td><td></td><td>SKL-S</td><td>GPP_B10</td></td<>			SKL-S	GPP_B10
Assign the CLKREQ# signal associated with CLKOUT_SRC5. SKL-0 NA SRC7 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-U NA SRC8 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-U NA SRC8 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-U NA SRC9 CLKREQ# mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-U NA SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SRC10 CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SRC10 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKL-Y NA SKL-Y NA SKL-Y SKL-Y SKL-Y NA SKL-Y NA SKL-Y NA SKL-Y		SRC6 CLKREQ# Mapping	SKL-Y	NA
SRC1 CLKREQ# Mapping SKL-S GPP_H0 SRC7 CLKREQ# Mapping SKL-S GPP_H0 Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-V NA SRC8 CLKREQ# Mapping SKL-H GPP_H1 SRC8 CLKREQ# Mapping SKL-V NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-V NA SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-V NA SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-V NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKL-S GPP_H3 SKL-S GPP_H43 SKL-S GPP_H43 SKL-Y NA		Assign the CERREQ# signal associated with CEROUT_SRC0.	SKL-U SKL-H	GPP HO
SRC7 CLKREQ# Mapping SRL V NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-Y NA SRC8 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-W NA SRC8 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-V NA SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-V NA SRC10 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-V NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKL-S GPP_H43 SKL-Y NA SKL-S GPP_H43 SKL-Y NA			SKL-N	GPP_H0
Assign the CLKREQ# signal associated with CLKOUT_SRC7. SKL-U NA SKL-H GPP_H1 SKL-S GPP_H1 SKL-S GPP_H1 SKL-S GPP_H1 SKL-S GPP_H2 SKL-U NA SKL-H GPP_H2 SKL-S GPP_H2 SKL-S GPP_H2 SKL-S GPP_H2 SKL-S GPP_H2 SKL-S GPP_H3 SKL-V NA SKL-H GPP_H3 SKL-S GPP_H3 SKL-S GPP_H3 SKL-S GPP_H4		SRC7 CLKREO# Mapping	SKL-Y	NA
SRC8 CLKREQ# Mapping SKL-H GPP_H1 Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-Y NA SRC9 CLKREQ# signal associated with CLKOUT_SRC8. SKL-U NA SRC9 CLKREQ# signal associated with CLKOUT_SRC8. SKL-H GPP_H2 SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-V NA SRC10 CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKL-H GPP_H3 SKL-H GPP_H4 SKL-S GPP_H4 SKL-S GPP_H4		Assign the CLKREQ# signal associated with CLKOUT SRC7.	SKL-U	NA
SRC8 CLKREQ# Mapping SKL-S GPP_H1 Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-V NA SKL-S GPP_H2 SKL-S GPP_H3 SKL-S GPP_H3 SKL-S GPP_H3 SKL-S GPP_H3 SKL-S GPP_H4 SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKL-S SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y SKL-H GPP_H4 SKL-Y NA			SKL-H	GPP_H1
SRC8 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-U NA SKL-S GPP_H2 SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SRC9 CLKREQ# mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-U NA SKL-S GPP_H3 SKL-S GPP_H3 SKL-S GPP_H3 SKL-S GPP_H3 SKL-S GPP_H4 Skign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-V NA Skign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-U NA Skign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-U NA Skign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-H GPP_H4 Skil-N GPP_H4 SKL-S GPP_H4			SKL-S	GPP_H1
Assign the CLKREQ# signal associated with CLKOUT_SRC8. SKL-U NA SRC9 CLKREQ# Mapping SKL-S GPP_H2 Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-V NA SRC9 CLKREQ# signal associated with CLKOUT_SRC9. SKL-U NA SKL-U NA SKL-U NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-U NA SKL-S GPP_H3 SKL-S GPP_H3 SRC10 CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKIP SKL-U NA SKL-Y Assign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-U NA SKL-H GPP_H4 GPP_H4		SRC8 CLKREQ# Mapping	SKL-Y	NA
SRC9 CLKREQ# Mapping SKL-H GPP_H2 Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SKL-H GPP_H3 SKL-H GPP_H3 SKL-S GPP_H3 SKL-S GPP_H3 SRC10 CLKREQ# mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKIL SKL-S GPP_H3 SKL-S GPP_H4 SKL-H GPP_H4		Assign the CLKREQ# signal associated with CLKOUT_SRC8.	SKL-U	NA
SRC9 CLKREQ# Mapping SKL-S GPP_H2 Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-Y NA SKL-H GPP_H3 SKL-S GPP_H3 SKL-S GPP_H3 SKL-S GPP_H3 SKL-W NA SKL-S GPP_H3 SKL-S GPP_H3 SKL-S GPP_H4 SKL-W NA			SKL-H	GPP_H2
SRC9 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-U NA SKL-H GPP_H3 SKL-S GPP_H3 SRC10 CLKREQ# Mapping SKL-Y NA Assign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-Y NA SKL-H GPP_H3 GPP_H4 SKL-S GPP_H4 SKL-Y			SKL-S	GPP_H2
Assign the CLKREQ# signal associated with CLKOUT_SRC9. SKL-U NA SKL-B GPP_H3 SKL-S GPP_H3 SRC10 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-U NA SKL-U NA SKL-H GPP_H4 SKL-S GPP_H4		SRC9 CLKREQ# Mapping	SKL-Y	NA
SRC10 CLKREQ# Mapping SKL-H GPP_H3 Assign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-V NA SKL-H GPP_H4 SKL-H SKL-H GPP_H4		Assign the CLKREQ# signal associated with CLKOUT_SRC9.	SKL-U	
SRC10 CLKREQ# Mapping SKL-3 GFP_FI3 Assign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-V NA SKL-H GPP_H4 SKL-S GPP_H4			SKL-H	
Assign the CLKREQ# signal associated with CLKOUT_SRC10. SKL-U NA SKL-H GPP_H4 SKL-S GPP_H4		SPC10 CLKPEO# Manning	SKL-S	
SKL-H GPP_H4 SKL-S GPP_H4		Assign the CLKREO# signal associated with CLKOUT_SRC10	SKI-U	NA
SKL-S GPP_H4			SKL-H	GPP_H4
			SKL-S	GPP_H4



#	Parameter	Platform	Settings
	SRC11 CLKREQ# Mapping	SKL-Y	NA
	Assign the CLKREQ# signal associated with CLKOUT_SRC11.	SKL-U	NA
		SKL-H	GPP_H5
		SKL-S	GPP_H5
	SRC12 CLKREQ# Mapping	SKL-Y	NA
	Assign the CLKREQ# signal associated with CLKOUT_SRC1.	SKL-U	NA
		SKL-H	GPP_H6
		SKL-S	GPP_H6
	SRC13 CLKREQ# Mapping	SKL-Y	NA
	Assign the CLKREQ# signal associated with CLKOUT_SRC13.	SKL-U	NA
		SKL-H	GPP_H7
		SKL-S	GPP_H7
	SRC14 CLKREQ# Mapping	SKL-Y	NA
	Assign the CLKREQ# signal associated with CLKOUT_SRC14.	SKL-U	NA
		SKL-H	GPP_H8
		SKL-S	GPP_H8
	SRC15 CLKREQ# Mapping	SKL-Y	NA
	Assign the CLKREQ# signal associated with CLKOUT_SRC15.	SKL-U	NA
		SKL-H	GPP_H9
		SKL-S	GPP_H9
	CLKREQ SRC0 [5:0] Enable	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
	control by the assigned CLKREQ# for CLKOUT_SRC[5:0]	SKL-S	Enabled
	CLKREQ SRC [15:6] enable - SKL-H Only		
	This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC[15:6]		
	CLKREQ SRC1 Enable	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
	control by the assigned CLKREQ# for CLKOUI_SRC1.	SKL-S	Enabled
	CLKREQ SRC2 Enable	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
	control by the assigned CLKREQ# for CLKOUT_SRC2.	SKL-S	Enabled
	CLKREQ SRC3 Enable	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
	CONTROL BY THE ASSIGNED CLKREQ# TOT CLKOUT_SRC3.	SKL-S	Enabled
	CLKREQ SRC4 Enable	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
		SKL-S	Enabled
	CLKREQ SRC5 Enable	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
	CONTROL BY THE ASSIGNED CLKREQ# TOP CLKOUT_SRC5.	SKL-S	Enabled
	CLKREQ SRC6 Enable	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	I his parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
L	Control by the assigned CERREQ# TO CERCUT_SRCO.	SKL-S	Enabled
	CLKREQ SRC7 Enable	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	I his parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
	CONTO BY THE ASSIGNED CERRER TO CEROUT_SRC7.	SKL-S	Enabled

Table 2-8. Intel[®] FIT - Integrated Clock Controller (Sheet 10 of 13)



Table 2-8. Intel[®] FIT - Integrated Clock Controller (Sheet 11 of 13)

#	Parameter	Platform	Settings
	CLKREQ SRC8 Enable	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
	control by the assigned CLKREQ# for CLKOUT_SRC8.	SKL-S	Enabled
	CLKREQ SRC9 Enable	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
	control by the assigned CLKREQ# for CLKOUT_SRC9.	SKL-S	Enabled
	CLKREQ SRC10 Enable	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
	control by the assigned CLKREQ# for CLKOUT_SRC10.	SKL-S	Enabled
	CLKREQ SRC11 Enable	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
	control by the assigned CLKREQ# for CLKOUT_SRCTT.	SKL-S	Enabled
	CLKREQ SRC12 Enable	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
	control by the assigned CLKREQ# for CLKOU1_SRC12.	SKL-S	Enabled
	CLKREQ SRC13 Enable	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
	control by the assigned CLKREQ# for CLKOUT_SRCT3.	SKL-S	Enabled
	CLKREQ SRC14 Enable	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
		SKL-S	Enabled
	CLKREQ SRC15 Enable	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
	This parameter allows user to Enable/Disable the dynamic clock request	SKL-H	Enabled
		SKL-S	Enabled
		SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	I his parameter allows user to Enable/Disable CLKRUN protocol on LPC1	SKL-H	Enabled
		SKL-S	Enabled
	CLKRUN LPC1 Enable	SKL-Y	Enabled
	This parameter allows user to Enable/Disable (LKDUN protocol on LDC1	SKL-U	Enabled
	output clock.	SKL-H	Enabled
		SKL-S	Enabled
	Voluce: Enchlad (Disabled	SKL-Y	Enabled
	This parameter decides if Crystal is forced to be on or is subjected to	SKL-U	
	dynamic shutdown. Crystal Oscillator can dynamically shut down upon	SKL-FI	Enabled
	iSCLK detecting idle condition on all clock consumers of crystal clock.	JKL-3	LIANEU
	Note: Recommendation is to leave setting at default value.		
	Clock Gating of CLKOUT_ITPxDP Disable	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	This parameter allows user to Enable/Disable dynamic control of	SKL-H	Enabled
	CLKOUT_ITPxDP.When enabled, CLKOUT_ITPxDP is subject to gating/ ungating control by CPUBCLKREQ	SKL-S	Enabled
	Note: Recommendation is to leave setting at default value.		



Table 2-8.	Intel [®] FIT -	Integrated	Clock Controller	(Sheet 12 of 13)
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#	Parameter	Platform	Settings
	Clock Gating of CLKOUT_CPUBCLK Disable	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	This parameter allows user to Enable/Disable dynamic control of	SKL-H	Enabled
	CLKOUT_CPUBCLK.When enabled, CLKOUT_CPUBCLK is subject to gating/	SKL-S	Enabled
	These settings should match with platform		
	hardware decign		
	Note: Decommendation is to leave setting at default value		
		SKI V	ΝΑ
		SKL-1	
	This parameter allows user to Enable/Disable dynamic control of	SKL-U	Enabled
	CLKOUT CPUPCIBCLK. When enabled. CLKOUT CPUPCIBCLK is subject to	SKL-N	Enabled
	gating/ungating control by CPUPCIBCLKREQ	SRE-5	LINDEO
	Note: Recommendation is to leave setting at default value.		
	Clock Gating of CLKOUT_CPUNSSC Disable	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	This parameter allows user to Enable/Disable dynamic control of	SKL-H	Enabled
	CLKOUT_CPUNSSC.When enabled, CLKOUT_CPUNSSC is subject to gating/	SKL-S	Enabled
	Note: Recommendation is to leave setting at default value		
		SKI V	Enabled
		SKL-II	Enabled
	This parameter allows user to Enable/Disable dynamic control of	SKL-U SKL-H	Enabled
	CLKOUT_CPUNSSC[P/N] .Controls the parked state of True (P) and	SKL-S	Enabled
	Complementary (N) copies of the differential pair when	0112 0	Lindbiod
	CLKOUT_CPUNSSC[P/N] is dynamically gated under S0 idle state.		
	Note: Recommendation is to leave setting at default value.		
	Clock Gating of icc_rosc_fast_clk Disable	SKL-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	I his parameter allows user to Enable/Disable dynamic clock gate on	SKL-H	Enabled
	Note: Recommendation is to leave setting at default value	SKL-S	Enabled
	Clock Gating of icc. rosc. side clk Disable	SKI-Y	Enabled
	Values: Enabled/Disabled	SKL-U	Enabled
	This parameter allows user to Enable/Disable dynamic clock gate on	SKL-H	Enabled
	icc_rosc_side_clk	SKL-S	Enabled
	Note: Recommendation is to leave setting at default value.		
	USB3Gen2PCI e PLL OFF Wait	SKL-Y	8us
	This parameter allows user to set G2PLLOFFWAIT timer value. Once timer	SKL-U	8us
	expires and there are no wake events, the USB3Gen2PCIe PLL can be	SKL-H	8us
	Note: Decommondation is to leave setting at default value	SKL-S	8us
		CKL V	0.00
	This parameter allows user to set G2PLL PGWAIT timer value. Once timer	SKL-1	ous
	expires and there are no wake events, the USB3Gen2PCIe PLL can be	SKL-U	803
	shutdown	SKL-S	803
	Note: Recommendation is to leave setting at default value.	SIL S	043
	Run-time SO SUS PG Wait	SKL-Y	8us
	This parameter allows user to set SUSPGWAIT timer value. Once timer	SKL-U	8us
	expires and there are no wake events, the USB3Gen2PCIe PLL can be	SKL-H	8us
	Note: Recommendation is to leave setting at default value	SKL-S	8us
1	note. Recommendation is to leave setting at default value.	1	



Table 2-8. Intel[®] FIT - Integrated Clock Controller (Sheet 13 of 13)

#	Parameter	Platform	Settings
	Crystal Oscillator Fast Restart Mode	SKL-Y	01b
	This parameter allows user to configure Crystal Oscillator Fast Restart	SKL-U	01b
	Mode. In all below listed fast start modes, iSCLK kickstarts crystal XIN/	SKL-H	01b
	XOUT by injecting a 24Mhz kickstart reference clock onto these pins.	SKL-S	01b
	Note: Configuration of this parameter co-relates to configuration of Clock Gating of Core 24MHz Crystal Disable parameter .		
	If Clock Gating of Core 24MHz Crystal Disable is set to 'Disable' , Crystal Oscillator Fast Restart Mode parameter has no impact .		
	If Clock Gating of Core 24MHz Crystal Disable is set to 'Enabled' , Crystal Oscillator Fast Restart Mode parameter must be set to '01b '. Other value like '00b' can cause wake latency conflict which can cause platform functional issue.		
	BCLK PLL Shutdown Wait Interval	SKL-Y	8us
	This parameter allows user to enable Dynamic power management of BCLK	SKL-U	8us
	PLL. Upon the event that all conditions (other than this wait timer itself)	SKL-H	8us
	are satisfied for ISCLK dynamic PLL shutdown, a timer is started. Unce it	SKL-S	8us
	Note: Recommendation is to leave setting at default value.		
	24MHz Crystal Shutdown Wait Interval	SKL-Y	8us
	This parameter allows user to Enable Dynamic power management of	SKL-U	8us
	Crystal. Upon the event that all conditions (other than this wait timer itself)	SKL-H	8us
	are satisfied for iSCLK crystal shutdown, a timer is started. Once it expires and there are no wake events, iSCLK will shutdown crystal		8us
	Note: Recommendation is to leave setting at default value.		



Table 2-9. Intel[®] FIT - Intel[®] Networking & Connectivity (Sheet 1 of 3)

1

Click on Networking & Connectivity in the left tabs menu> Wired LAN Configuration is expanded by default:

Wired LAN Configuration

Parameter	Value	Help Text
GbE MAC SMBus Address	0x70	-
GbE MAC SMBus Address En	Yes	This enables the Intel(R) Integrated Wired LAN MAC SMBus add
Intel(R) PHY over PCIe Enabled	Yes	This setting allows customers to enable / disable Intel(R) Integrat
GbE PCle Port Select	PORT5	This setting allows customers to configure the PCle Port that will
GbE PHY SMBus Address	0x64	This setting configures Intel(R) Integrated Wired LAN SMBus ad
LAN Power Well	SLP_LAN#	This setting allows customers to configure the powerwell that will
LAN PHY Power Control GPD1	LANPHYPC	This setting allows the to assign the LAN PHY Power Control sig
LAN PHY Power Up Time	100ms	-
Intel(R) Integrated Wired LAN	Disabled	-
PHY Connection	PHY on SMLink0	-

#	Parameter	Platform	Settings
	Networking & Connectivity - Wired LAN Configuration		
1			
	GbE MAC SMBus Address	SKL-Y	0x70
		SKL-U	0x70
		SKL-H	0x70
		SKL-S	0x70
	GbE SMBus Address Enabled	SKL-Y	Yes
	Values: Yes/No - This enables the Intel® Integrated Wired LAN MAC	SKL-U	Yes
	SMBus address. Note: This setting must be enabled if using Intel®	SKL-H	Yes
	Integrated LAN.	SKL-S	Yes
	Intel® PHY over PCIe Enabled	SKL-Y	Yes
	Values: Yes/No - This setting allows customers to enable / disable Intel $\ensuremath{\mathbb{R}}$	SKL-U	Yes
	Integrated LAN operation over the PCIe Port selected by the GbE PCIe Port Select option.	SKL-H	Yes
		SKL-S	Yes
	GbE PCI e Port Select	SKL-Y	PORT5
	Values: PORT3, PORT4, PORT5, PORT9, PORT10 - This setting allows customers to configure the PCIe Port that will Intel® Integrated LAN will operate on.	SKL-U	PORT4
		SKL-H	PORT5
		SKL-S	PORT5
	GbE PHY SMBus Address	SKL-Y	0x64
	This setting configures Intel® Integrated Wired LAN SMBus address to	SKL-U	0x64
	accept SMBus cycles from the MAC. Note: Recommended setting is 64h.	SKL-H	0x64
		SKL-S	0x64
	LAN Power Well	SKL-Y	SLP_LAN#
	Values: Core Well, Sus Well, ME Well, SLP_LAN - This setting allows	SKL-U	SLP_LAN#
	customers to configure the power well that will be used by Intel®	SKL-H	SLP_LAN#
	Note: Decommonded setting is SLP ANI#	SKL-S	SLP_LAN#
	Note: Recommended Setting is SLP_LAN#.		



Table 2-9. Intel[®] FIT - Intel[®] Networking & Connectivity (Sheet 2 of 3)

2

#	Parameter	Platform	Settings	
	LAN PHY Power Control GPD11 Signal Configuration	SKL-Y	LANPHYPC	
	Values: GPD11, LANPHYPC - This setting allows the customer to assign	SKL-U	LANPHYPC	
	the LAN PHY Power Control signal to GbE or as GDP11. Note: If using	SKL-H	LANPHYPC	
	Intel® Integrated LAN this setting should be set to "Enable as LANPHYPC".	SKL-S	LANPHYPC	
	LAN PHY Power Up Time	SKL-Y	100ms	
	Values: 50ms, 100ms	SKL-U	100ms	
		SKL-H	100ms	
		SKL-S	100ms	
	Intel® Integrated Wired LAN Enable	SKL-Y	Enabled	
	Values: Enabled/Disabled - This setting enables or disables the Intel® Integrated LAN.	SKL-U	Enabled	
		SKL-H	Enabled	
		SKL-S	Enabled	
	PHY Connection	SKL-Y	PHY on SMLink0	
	Values: No PHY connected, PHY on SMLink0	SKL-U	PHY on SMLink0	
		SKL-H	PHY on SMLink0	
		SKL-S	PHY on SMLink0	
Click or	n Networking & Connectivity in the left tabs menu> Wireless LAN Con	figuration is expa	anded by default:	

Wireless LAN Configuration

Parameter	Value	Help Text		
Intel (R) ME CLINK Signal Enabled Yes This setting		This setting allows customers to enable / disable the Wirel		
MLK_RSTB Buffer Driven Mode	Open-drained	This soft strap determines the control mode for the output		
WLAN Microcode	0x24F3 SNOWFIELD	This setting allows OEMs to configure which Intel(R) Wirele		
WLAN Power Well	SLP_WLAN#	This setting allows customers to configure the powerwell t		
SLP_WLAN# / GPD9 Signal Con	SLP_WLAN#	This setting allows the user to assign the WLAN Powe		

#	Parameter	Platform	Settings
	Networking & Connectivity - Wireless LAN Configuration		
2			
	CLINK Enabled	SKL-Y	YesNo
	Values: Yes/No - This setting allows customers to enable / disable the Wireless LAN CLINK signal through Intel® ME firmware. Note: For using	SKL-U	YesNo
		SKL-H	YesNo
	Inter® vero wireless solutions this should be set to yes .	SKL-S	YesNo
	MLK_RSTB Buffer Driven Mode	SKL-Y	NA
	Values: Open-drained/Driven - This soft strap determines the control	SKL-U	NA
	mode for the output buffer MLK_RST # signal.	SKL-H	Driven
		SKL-S	Driven
	WLAN Microcode - This setting allow OEMs to configure which Intel®	SKL-Y	0x24F3
	Wireless LAN card microcode to load into the firmware image.	SKL-U	0x24F3
		SKL-H	0x24F3
		SKL-S	0x24F3



Table 2-9. Intel[®] FIT - Intel[®] Networking & Connectivity (Sheet 3 of 3)

#	Parameter			Platform	Settings		
-	WLAN Power Well			SKL-Y	SLP_WLAN#		
	Values: Disabled, Sus Well, ME Well, SLP_M# SPDA, SLP_WLAN#			SKL-U	SLP_WLAN#		
	- This setting allows	OEMs to configure the power	well that will be used by	SKL-H	SLP_WLAN#		
	Intel® Wireless LAN			SKL-S	SLP_WLAN#		
	WLAN Sleep via SLF	2_WLAN# (default)					
	Note: Recommende	ed setting is SLP_WLAN#.					
	SLP_WLAN# / GP	D9 Signal Configuration		SKL-Y	SLP_WLAN#		
	Values: SLP_WLAN#, GPD9 - This setting allows the customer to assign			SKL-U	SLP_WLAN#		
	Intel® Wireless I AN	I this setting should be set to	"Enable as SLP_WLAN#"	SKL-H	SLP_WLAN#		
	The wireless LAN this setting should be set to "Linable as SEF_WLAN# .			SKL-S	SLP_WLAN#		
Click or	n Networking & Cor	nectivity in the left tabs m	nenu> Intel® NFC Config	juration is expan	ded by default:		
	Intel (R) NFC Configuration						
	Parameter Value H			elp Text			
Enable N	Enable Near Field Communica No -						
NFC SM	NFC SMBus Address 0x28-NXP -						
#		Parameter		Platform	Settings		
3	Networking & Connectivity Intel® NFC Configuration						
	Enable Near Field Communication		SKL-Y	Yes			
	Values: Yes/No - This setting allows OEMs to enable / disable Near Field		SKL-U	Yes			
	Communication support in the Intel® ME firmware.		SKL-H	No			
	Note: If NFC device set to No, as it can	te: If NFC device is not in the system configuration, leave this setting to No, as it can cause BIST testing to fail.		SKL-S	No		
	NFC SMBus Address			SKL-Y	0x29-NXP		
	Values: 0x28-NXP, 0x29-NXP, 0x2A-NXP, 0x2B-NXP - This setting allows OEMs to configure the SMBus address for the NFC adapter being used.		SKL-U	0x29-NXP			
			SKL-H	0x28-NXP			
			SKL-S	0x29-NXP			



Table 2-10. Intel[®] FIT - Flex I/O (Sheet 1 of 10)

Click on Flex I/O in the left tabs menu> Intel® RST for PCIe Configuration is expanded by default:

 Interview 	el(R) RST for PCIe	Configuration 1				
	Parameter	Value		Help Text		
ntel(R) R	ST for PCIe-C1 Selec	x2	This is used to configure N	AND Cycle routers for the	he Intel(R) RS	
ntel(R) R	ST for PCIe-C2 Selec	x2	This is used to configure N	AND Cycle routers for the	he Intel(R) RS	
ntel(R) R	ST for PCIe-C3 Selec	x2	This is used to configure NAND Cycle routers for the Intel(R) RS			
ntel(R) R	ST for PCle Controller 1	2x2	This is used to configure P	Cle Controller 1 for Inte	I(R) RST for P	
ntel(R) R	ST for PCle Controller 2	2x2	This is used to configure P	Cle Controller 2 for Inte	I(R) RST for P	
ntel(R) R	ST for PCIe Controller 3	2x2	This is used to configure P	Cle Controller 3 for Inte	I(R) RST for P	
PCle Cor	ntroller 3 Port 1 SRIS	No	This is used to configure S	RIS Port 1 for Intel(R) F	RST for PCIe o	
PCle Cor	ntroller 3 Port 2 SRIS	No	This is used to configure S	RIS Port 2 for Intel(R) F	RST for PCle o	
PCle Cor	Controller 3 Port 3 SRIS No This is used to configure SRIS Port 3 for Intel(R) RST for PCIe o.			RST for PCle o		
PCle Cor	Controller 3 Port 4 SRIS No This is used to configure SRIS Port 4 for Intel(R) RST for PCIe o.			RST for PCle o		
PCle Cor	controller 4 Port 1 SRIS No This is used to configure SRIS Port 1 for Intel(R) RST for PCIe o.			RST for PCIe o		
PCle Cor	Controller 4 Port 2 SRIS No This is used to configure SRIS Port 2 for Intel(R) RST for PCIe o.			RST for PCIe o		
PCle Cor	Controller 4 Port 3 SRIS No This is used to configure SRIS Port 3 for Intel(R) RST for PCIe o			RST for PCIe o		
PCle Cor	Controller 4 Port 4 SRIS No This is used to configure SRIS Port 4 for Intel(R) RST for PCIe o.			RST for PCIe o		
PCle Cor	ntroller 5 Port 1 SRIS	roller 5 Port 1 SRIS No This is used to configure SRIS Port 1 for Intel(R) RST for PCIe o			RST for PCIe o	
PCle Cor	ntroller 5 Port 2 SRIS No This is used to configure SRIS Port 2 for Intel(R) RST for PCIe o			RST for PCIe o		
PCIe Cor	ntroller 5 Port 3 SRIS	No	This is used to configure SRIS Port 3 for Intel(R) RST for PCIe o			
PCle Cor	ntroller 5 Port 4 SRIS	No	This is used to configure S	RIS Port 4 for Intel(R) F	RST for PCIe o	
#		Parameter		Platform	Settin	
0	Flex I/C) - Intel® RST for PCIe Co	nfiguration			
	Intel® RST for PCIe-C1 Select x2 or x4		Cycle routers for the	SKL-Y	NA	
	values: x2, x4 - This is used to configure NAND Cycle routers for the Intel® RST for PCIe interface as either x2 or x4 lane operation on PCIe		SKL-H	x2		
	Controller 1.		SKL-S	x2		
	Values: x2, x4 - This is used to configure NAND Cycle routers for the		SKL-U	x2 x2		
	Intel® RST for PCIe interface as either x2 or x4 lane operation on PC Controller 2.		ane operation on PCIe	SKL-H	x2	
				SKL-S	x2	
	Intel® RST for PCI	Ie-C3 Select x2 or x4	Cuelo routors for the	SKL-Y	x2	
	Values: x2, x4 - This is used to configure NAND Cycle routers for the Intel® RST for PCIe interface as either x2 or x4 lane operation on PCIe Controller 3.		ane operation on PCIe	SKL-U SKL-H	X4 X4	
			•			

SKL-S



Table 2-10. Intel[®] FIT - Flex I/O (Sheet 2 of 10)

#	Parameter	Platform	Settings
	Intel® RST for PCIe Controller 1	SKL-Y	NA
	Values: 1x4, 2x2 - This is used to configure PCIe Controller 1 for	SKL-U	NA
	Intel® RST for PCIe interface as either x2 or x4 lane operation on PCIe	SKL-H	x2
	Controller 1.	SKL-S	x2
	Intel® RST for PCIe Controller 2	SKL-Y	x2
	Values: 1x4, 2x2 - This is used to configure PCIe Controller 2 for	SKL-U	x2
	Intel® RST for PCIe interface as either x2 or x4 lane operation on PCIe	SKL-H	x2
	Controller 2.	SKL-S	x2
	Intel® RST for PCIe Controller 3	SKL-Y	x2
	Values: 1x4, 2x2 - This is used to configure PCIe Controller 3 for	SKL-U	x4
	Intel® RST for PCIe interface as either x2 or x4 lane operation on PCIe	SKL-H	x4
	Controller 3.	SKL-S	x4
	PCIe Controller 2 Port 1 SRIS Enabled	SKL-Y	No
	Values: Yes/ No - This is used to configure SRIS Port 1 for Intel® RST	SKL-U	No
	for PCIe on PCIe Controller 2. Note: Configuration of this setting is only	SKL-H	No
	cable	SKL-S	No
-	PCIe Controller 2 Port 2 SPIS Enabled	SKI-V	No
	Values: Yes/ No - This is used to confidure SRIS Port 2 for Intel® RST	SKL-U	No
	for PCIe on PCIe Controller 2. Note: Configuration of this setting is only	SKI-H	No
	required if the NVM device will be connected external SATA Express	SKL-S	No
	cable.	0112 0	
	PCIe Controller 2 Port 3 SRIS Enabled	SKL-Y	No
	Values: Yes/ No - This is used to configure SRIS Port 3 for Intel® RST for PCIe on PCIe Controller 2. Note: Configuration of this setting is only	SKL-U	No
	required if the NVM device will be connected external SATA Express	SKL-H	No
	cable.	SKL-S	No
	PCIe Controller 2 Port 4 SRIS Enabled	SKL-Y	No
	Values: Yes/ No - This is used to configure SRIS Port 4 for Intel® RST for PCIe on PCIe Controller 2. Note: Configuration of this setting is only	SKL-U	No
		SKL-H	No
	cable.	SKL-S	No
	PCIe Controller 3 Port 1 SRIS Enabled	SKL-Y	No
	Values: Yes/ No - This is used to configure SRIS Port 1 for Intel® RST	SKL-U	No
	for PCIe on PCIe Controller 3. Note: Configuration of this setting is only	SKL-H	No
	cable.	SKL-S	No
	PCIe Controller 3 Port 2 SRIS Enabled	SKI-Y	No
	Values: Yes/ No - This is used to configure SRIS Port 2 for Intel® RST	SKL-U	No
	for PCIe on PCIe Controller 3. Note: Configuration of this setting is only	SKL-H	No
	required if the NVM device will be connected external SATA Express	SKL-S	No
	Cable.	CKL V	N-
	Value: Vec / No. This is used to configure CDIS Dert 2 for Intel® DST.	SKL-I	No
	for PCIe on PCIe Controller 3. Note: Configuration of this setting is only		No
	required if the NVM device will be connected external SATA Express	SKL-II	No
	cable.	JRE-5	110
	PCIe Controller 3 Port 4 SRIS Enabled	SKL-Y	No
	Values: Yes/No - This is used to configure SRIS Port 4 for Intel® RST	SKL-U	No
	required if the NVM device will be connected external SATA Express	SKL-H	No
	cable.	SKL-S	No
	PCIe Controller 4 Port 1 SRIS Enabled	SKL-Y	NA
	Values: Yes/ No - This is used to configure SRIS Port 1 for Intel® RST	SKL-U	NA
	for PCIe on PCIe Controller 4. Note: Configuration of this setting is only	SKL-H	No
	cable.	SKL-S	No
	PCIe Controller 4 Port 2 SRIS Enabled	SKI-Y	NA
	Values: Yes/ No - This is used to configure SRIS Port 2 for Intel® RST	SKI-U	NA
	for PCIe on PCIe Controller 4. Note: Configuration of this setting is only	SKL-H	No
	required if the NVM device will be connected external SATA Express	SKL-S	No
	cable.	SILE O	


Table 2-10. Intel[®] FIT - Flex I/O (Sheet 3 of 10)

#	Parameter		Platform	Settings		
	PCIe Controller 4	Port 3 SRIS Enabled		SKL-Y	NA	
	Values: Yes/ No -	This is used to configure SRIS	Port 3 for Intel® RST	SKL-U	NA	
	for PCIe on PCIe Cor	ntroller 4. Note: Configuration	n of this setting is only	SKL-H	No	
	cable.	device will be connected exter	nai SATA EXPRESS	SKL-S	No	
	PCIe Controller 4	Port 4 SRIS Enabled		SKL-Y	NA	
	Values: Yes/No - This is used to configure SRIS Port 4 for Intel® RST			SKL-U	NA	
	required if the NVM device will be connected external SATA Express			SKL-H	No	
	cable.	device will be connected exten	That SATA Express	SKL-S	No	
	PCIe Controller 5	Port 1 SRIS Enabled		SKL-Y	NA	
	Values: Yes/ No -	This is used to configure SRIS	Port 1 for Intel® RST	SKL-U	NA	
	for PCIe on PCIe Cor	ntroller 5. Note: Configuration	n of this setting is only	SKL-H	No	
	cable.	device will be connected exter	Har SATA Express	SKL-S	No	
	PCIe Controller 5	Port 2 SRIS Enabled		SKL-Y	NA	
	Values: Yes/ No -	This is used to configure SRIS	Port 2 for Intel® RST	SKL-U	NA	
	for PCIe on PCIe Cor	ntroller 5. Note: Configuration	n of this setting is only	SKL-H	No	
	cable.	aevice will be connected exter	mai SATA Express	SKL-S	No	
	PCIe Controller 5	Port 3 SRIS Enabled		SKL-Y	NA	
	Values: Yes/ No -	This is used to configure SRIS	Port 3 for Intel® RST	SKL-U	NA	
	for PCIe on PCIe Cor	ntroller 5. Note: Configuratior	n of this setting is only	SKL-H	No	
	required if the NVM cable.	device will be connected exter	rnal SATA Express	SKL-S	No	
	PCIe Controller 5	Port 4 SRIS Enabled		SKL-Y	NA	
	Values: Yes/ No -	This is used to configure SRIS	Port 4 for Intel® RST	SKL-U	NA	
	for PCIe on PCIe Cor	ntroller 5. Note: Configuration	n of this setting is only	SKL-H	No	
	required if the NVM	device will be connected exter	rnal SATA Express	SKL-S	No	
Click or	Flex I/O in the lef	t tabs menu> PCIe Lane Re	eversal Configuration	is expanded by d	efault:	
▼ P(Cle Lane Reversal C	Configuration	2		·	
	Parameter	Value		Help Text		
PCle Co	ontroller 1 Lane Revers	No	This setting allows the PC	le lanes on Controller 1 to be reversed		
PCIe Co	ontroller 2 Lane Revers	No	This setting allows the PC	le lanes on Controller 2 to be reversed		
PCIe Co	ontroller 3 Lane Revers	No	This setting allows the PCI	le lanes on Controller 3 to be reversed		
PCle Co	ontroller 4 Lane Revers	No	This setting allows the PCI	le lanes on Controller 4 to be reversed		
PCIe Co	ontroller 5 Lane Revers	No	This setting allows the PC	e lanes on Controller 5	to be reversed	
#		Parameter		Platform	Settings	
	Flex I/O - PCI e La	ne Reversal Configuration				
2						
	PCIe Controller 1 Lane Reversal Enabled		SKL-Y	No		
	Values: Yes/ No -	This setting allows the PCIe la	nes on Controller 1 to	SKL-U	No	
	be reversed. Note:	In order to use Lane Reversal	the PCIe Controller	SKL-H	No	
	Platform Controller	ed 1x4. For further details s Hub EDS.	ее экујаке н / ЦР	SKL-S	No	
	PCIe Controller 2	Lane Reversal Enabled		SKL-Y	No	
	Values: Yes/ No -	This setting allows the PCIe la	ines on Controller 2 to	SKL-U	No	
	be reversed. Note:	In order to use Lane Reversal	the PCIe Controller	SKL-H	No	
	needs to be configur	ed as 1x4. For further detail	s see Skylake H / LP	SKL-S	No	
	Platform Controller Hub EDS.					



Table 2-10. Intel[®] FIT - Flex I/O (Sheet 4 of 10)

#		Parameter			Settings
	PCIe Controller 3	Lane Reversal Enabled		SKL-Y	No
	Values: Yes/ No -	This setting allows the PCIe I	anes on Controller 3 to	SKL-U	Yes
	be reversed. Note:	In order to use Lane Reversa	I the PCIe Controller	SKL-H	No
	Platform Controller	irea as 1x4. For further detai	iis see Skylake H / LP	SKL-S	No
	Plation Controllor 4	stroller 4 Lane Deversal Enchlad		SVI V	ΝΔ
	Values: Ves / No - This setting allows the PCIe lanes on Controller 4 to			SKL-T	
	be reversed. Note:	be reversed Note: In order to use Lane Reversal the PCIe Controller			No
	needs to be configu	red as 1x4. For further detai	ils see Skylake H / LP	SKL-II	No
	Platform Controller	Hub EDS.		JKL-J	NO
	PCIe Controller 5	Lane Reversal Enabled		SKL-Y	NA
	Values: Yes/ No -	This setting allows the PCIe I	anes on Controller 5 to	SKL-U	NA
	be reversed. Note:	In order to use Lane Reversa	I the PCIe Controller	SKL-H	No
	Platform Controller	Hub EDS.	IIS SEE SKYIAKE H / LP	SKL-S	No
Click or	n Flex I/O in the lef	ft tabs menu> PCIe Port Co	onfiguration is expand	ed by default:	
▼ P(Cle Port Configurat	ion 3			
	Parameter	Value		Help Text	
PCle Co	ontroller 1 (Port 1-4)	1x4	This setting controls PCIe I	Port configurations for F	Cle Controller
PCle Co	ontroller 2 (Port 5-8)	4x1	This setting controls PCIe I	Port configurations for F	Cle Controller
PCle Co	ontroller 3 (Port 9-12)	4x1	This setting controls PCIe F	Port configurations for F	Cle Controller
PCle Co	ontroller 4 (Port 13-16)	2x2	This setting controls PCIe I	Port configurations for F	Cle Controller
PCle Co	PCIe Controller 5 (Port 17-20) 1x4 This setting controls PCIe		This setting controls PCIe I	Port configurations for F	Cle Controller
#		Parameter		Platform	Settings
	Flex I/O - PCIe P	ort Configuration			
3					
	PCIe Controller 1	(Port 1-4)		SKL-Y	1x4
	Values: 4x1, (1x2	2, 2x1), 2x2, 1x4 - This settin	ng controls PCIe Port	SKL-U	4x1
	LP Platform Control	ler Hub FDS	аетану see экунаке H /	SKL-H	1x4
	2. Hattorni oontrol			SKL-S	4x1
	PCIe Controller 2	(Port 5-8)		SKL-Y	4x1
	Values: 4x1, (1x2	2, 2x1), 2x2, 1x4 - This settin	ng controls PCIe Port	SKL-U	4x1
	LP Platform Control	Cie Controller 2. For further d	ietalis see Skylake H /	SKL-H	4x1
				SKL-S	4x1
	PCIe Controller 3	(Port 9-12)		SKL-Y	4x1
	Values: 4x1, (1x2	2, 2x1), 2x2, 1x4 - This settin	ng controls PCIe Port	SKL-U	1x4
	configurations for PCIe Controller 3. For further details see Skylake H /			SKL-H	4x1
	LP Platform Controller Hub EDS.			SKL-S	1x4
	PCIe Controller 4	(Port 13-16)		SKL-Y	NA
	Values: 4x1, (1x2	2, 2x1), 2x2, 1x4 - This settin	ng controls PCIe Port	SKL-U	NA
	configurations for P	Cle Controller 4. For further d	letails see Skylake H /	SKL-H	1x2, 2x1
	LP Platform Control			SKL-S	1x2, 2x1
	PCIe Controller 5	(Port 17-20)		SKL-Y	NA
	Values: 4x1, (1x2	2, 2x1), 2x2, 1x4 - This settin	ng controls PCIe Port	SKL-U	NA
	configurations for P	Cle Controller 5. For further d	letails see Skylake H /	SKL-H	4x1
	LP Platform Control	ler Hub EDS.		SKL-S	1x4



Table 2-10. Intel[®] FIT - Flex I/O (Sheet 5 of 10)

Click on Flex I/O in the left tabs menu> SATA / PCI e Combo Port Configuration is expanded by default:

Parameter	Value		Help Text	
SATA / PCIe Combo Port 0	SATA	This setting configures the	PCle port to operate	as either PCle P
SATA / PCIe Combo Port 1 GPIO		This setting configures the	PCIe port to operate	as either PCle P
SATA / PCIe Combo Port 2	PCIe (or GbE)	This setting configures the	PCle port to operate	as either PCle P
ATA / PCIe Combo Port 3	PCle (or GbE)	This setting configures the	PCle port to operate	as either PCle P
SATA / PCIe Combo Port 4	GPIO	This setting configures the	PCle port to operate	as either PCle P
SATA / PCIe Combo Port 5	GPIO	This setting configures the	PCle port to operate	as either PCle P
SATA / PCIe Combo Port 6	GPIO	This setting configures the	PCle port to operate	as either PCle P
SATA / PCIe Combo Port 7	PCle (or GbE)	This setting configures the	PCIe port to operate	as either PCle P
#	Parameter		Platform	Settings
Values: SATA, Porte Col	mbo Port 0 Cle (or GbE), GPIO - Th s either:	his setting configures the PCIe	SKL-Y SKL-U	SATA SATA
Values: SATA, Projection Values: SATA, Proport to operate as PCIe Port 7 or SA PCIe Port 9 or SA For further details	mbo Port 0 CIe (or GbE), GPIO - Th s either: TA Port 0 (LP) TA Port 0 (H) s on Flex I/O see Skylake	his setting configures the PCIe H / LP Platform Controller	SKL-Y SKL-U SKL-H SKL-S	SATA SATA SATA PCIe (or GbE)
Values: SATA / Pore Col Values: SATA, Pore port to operate as PCIe Port 7 or SA ^T PCIe Port 9 or SA ^T For further details Hub EDS. SATA / PCIe Col	mbo Port 0 Cle (or GbE), GPIO - Th s either: TA Port 0 (LP) TA Port 0 (H) s on Flex I/O see Skylake mbo Port 1	his setting configures the PCIe H / LP Platform Controller	SKL-Y SKL-U SKL-H SKL-S SKL-Y	SATA SATA SATA PCIe (or GbE) GPIO
Values: SATA / Pore Col Values: SATA, Po port to operate as PCIe Port 7 or SA PCIe Port 9 or SA For further details Hub EDS. SATA / PCIe Con Values: SATA, PC	mbo Port 0 CIe (or GbE), GPIO - Th s either: TA Port 0 (LP) TA Port 0 (H) s on Flex I/O see Skylake mbo Port 1 CIe (or GbE), GPIO - Th	his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe	SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U	SATA SATA SATA PCIe (or GbE) GPIO SATA
Values: SATA / Pcte Col Values: SATA, Pr port to operate as PCIe Port 7 or SA PCIe Port 9 or SA For further details Hub EDS. SATA / PCIe Con Values: SATA / PCIe Con Values: SATA / PCIe Con Values: SATA / PCIe Con	mbo Port 0 CIe (or GbE), GPIO - Th s either: TA Port 0 (LP) TA Port 0 (H) s on Flex I/O see Skylake mbo Port 1 CIe (or GbE), GPIO - Th s either: TA Port 1 (LP)	his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe	SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H	SATA SATA SATA PCIe (or GbE) GPIO SATA SATA
Values: SATA / PcTe Co Values: SATA, Pr port to operate as PCIe Port 7 or SA PCIe Port 9 or SA For further details Hub EDS. SATA / PCIe Con Values: SATA, P port to operate as PCIe Port 8 or SA PCIe Port 10 or S/ For further details Hub EDS.	mbo Port 0 CIe (or GbE), GPIO - Th s either: TA Port 0 (LP) TA Port 0 (H) s on Flex I/O see Skylake mbo Port 1 CIe (or GbE), GPIO - Th s either: TA Port 1 (LP) ATA Port 1 (H) s on Flex I/O see Skylake	his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe H / LP Platform Controller	SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S	SATA SATA SATA PCIe (or GbE) GPIO SATA SATA PCIe (or GbE)
Values: SATA / PCIe Col Values: SATA, Pv port to operate as PCIe Port 7 or SA PCIe Port 9 or SA For further details Hub EDS. SATA / PCIe Col Values: SATA, Pv port to operate as PCIe Port 8 or SA PCIe Port 10 or SA For further details Hub EDS. SATA / PCIe Col	mbo Port 0 CIe (or GbE), GPIO - Th s either: TA Port 0 (LP) TA Port 0 (H) s on Flex I/O see Skylake mbo Port 1 CIe (or GbE), GPIO - Th s either: TA Port 1 (LP) ATA Port 1 (H) s on Flex I/O see Skylake mbo Port 2	his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe H / LP Platform Controller	SKL-Y SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S SKL-Y	SATA SATA SATA PCIe (or GbE) GPIO SATA SATA PCIe (or GbE) PCIe (or GbE)
Values: SATA / PCIe Col Values: SATA, Pc port to operate as PCIe Port 7 or SA PCIe Port 9 or SA For further details Hub EDS. SATA / PCIe Col Values: SATA, PC port to operate as PCIe Port 8 or SA PCIe Port 10 or SA For further details Hub EDS. SATA / PCIe Col Values: SATA / PCIe Col Values: SATA / PCIe Col Values: SATA / PCIe Col Values: SATA / PCIe Col	mbo Port 0 CIe (or GbE), GPIO - Th s either: TA Port 0 (LP) TA Port 0 (H) s on Flex I/O see Skylake mbo Port 1 CIe (or GbE), GPIO - Th s either: TA Port 1 (LP) ATA Port 1 (H) s on Flex I/O see Skylake mbo Port 2 CIe (or GbE), GPIO - Th s either:	his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe H / LP Platform Controller	SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-H SKL-S SKL-Y SKL-U SKL-U	SATA SATA SATA PCIe (or GbE) GPIO SATA SATA PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) PCIe (or GbE)
Values: SATA, Perfection Values: SATA, Perfection Port to operate as PCIe Port 7 or SA PCIe Port 9 or SA For further details Hub EDS. SATA / PCIe Con Values: SATA, Perfection Port to operate as PCIe Port 8 or SA PCIe Port 10 or SA For further details Hub EDS. SATA / PCIe Con Values: SATA, Perfection Values: SATA, Perfection Values: SATA, Perfection Values: SATA, Perfection Port to operate as PCIE Port 11 or SA	mbo Port 0 CIe (or GbE), GPIO - Th s either: TA Port 0 (LP) TA Port 0 (H) s on Flex I/O see Skylake mbo Port 1 CIe (or GbE), GPIO - Th s either: TA Port 1 (LP) ATA Port 1 (H) s on Flex I/O see Skylake mbo Port 2 CIe (or GbE), GPIO - Th s either: ATA Port 1 (LP)	his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe H / LP Platform Controller	SKL-Y SKL-U SKL-H SKL-S SKL-U SKL-H SKL-S SKL-U SKL-H SKL-H SKL-S	SATA SATA SATA PCIe (or GbE) GPIO SATA SATA PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) SATA
Values: SATA, Protection Values: SATA, Properties of the operate as PCIe Port 7 or SA PCIe Port 9 or SA For further details Hub EDS. SATA / PCIe Con Values: SATA, Properties of SA PCIe Port 8 or SA PCIe Port 10 or SA For further details Hub EDS. SATA / PCIe Con Values: SATA, Properties of SATA PCIE Port 10 or SA SATA / PCIE Con Values: SATA, Properties of SATA PCIE Port 11 or SA PCIE Port 13 or SA For further details Hub EDS.	mbo Port 0 CIe (or GbE), GPIO - Th s either: TA Port 0 (LP) TA Port 0 (H) s on Flex I/O see Skylake mbo Port 1 CIe (or GbE), GPIO - Th s either: TA Port 1 (LP) ATA Port 1 (H) s on Flex I/O see Skylake mbo Port 2 CIe (or GbE), GPIO - Th s either: ATA Port 1 (LP) ATA Port 1 (LP) ATA Port 1 (LP) ATA Port 0 (H) s on Flex I/O see Skylake	his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe H / LP Platform Controller	SKL-Y SKL-U SKL-H SKL-S SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-H SKL-S	SATA SATA SATA PCIe (or GbE) GPIO SATA SATA PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) SATA
Values: SATA, Prote Col Values: SATA, Pro- port to operate as PCIe Port 7 or SA PCIe Port 9 or SA For further details Hub EDS. SATA / PCIe Con Values: SATA, Pro- port to operate as PCIe Port 8 or SA PCIe Port 10 or S/ For further details Hub EDS. SATA / PCIe Con Values: SATA, Pro- port to operate as PCIe Port 11 or S/ PCIe Port 13 or S/ For further details Hub EDS. SATA / PCIe Con Values: SATA, PCIE Con SATA / PCIE Con	mbo Port 0 CIe (or GbE), GPIO - Th s either: TA Port 0 (LP) TA Port 0 (H) s on Flex I/O see Skylake mbo Port 1 CIe (or GbE), GPIO - Th s either: TA Port 1 (LP) ATA Port 1 (H) s on Flex I/O see Skylake mbo Port 2 CIe (or GbE), GPIO - Th s either: ATA Port 1 (LP) ATA Port 1 (LP) ATA Port 1 (LP) ATA Port 0 (H) s on Flex I/O see Skylake mbo Port 3	his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe H / LP Platform Controller	SKL-Y SKL-U SKL-H SKL-S SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S SKL-Y	SATA SATA SATA SATA PCIe (or GbE) GPIO SATA SATA PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) SATA PCIe (or GbE)
Values: SATA, Protection Values: SATA, Properties as PCIe Port 7 or SA PCIe Port 7 or SA For further details Hub EDS. SATA / PCIe Con Values: SATA, Properties as PCIe Port 8 or SA PCIe Port 8 or SA PCIe Port 10 or SA For further details Hub EDS. SATA / PCIe Con Values: SATA, Properties as PCIe Port 11 or SA PCIE Port 13 or SA PCIE Port 13 or SA PCIE Port 13 or SA For further details Hub EDS. SATA / PCIE Con Values: SATA, PCIE Con Values: SATA / PCIE Con	mbo Port 0 CIe (or GbE), GPIO - The s either: TA Port 0 (LP) TA Port 0 (H) s on Flex I/O see Skylake mbo Port 1 CIe (or GbE), GPIO - The s either: TA Port 1 (LP) ATA Port 1 (H) s on Flex I/O see Skylake mbo Port 2 CIe (or GbE), GPIO - The s either: ATA Port 1 (LP) ATA Port 1 (LP) ATA Port 1 (LP) ATA Port 1 (LP) ATA Port 0 (H) s on Flex I/O see Skylake mbo Port 3 CIe (or GbE), GPIO - The s either:	his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe H / LP Platform Controller	SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-U	SATA SATA SATA SATA PCIe (or GbE) GPIO SATA SATA PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) SATA PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) PCIe (or GbE)
Values: SATA / PCIe Col Values: SATA, Pr port to operate as PCIe Port 7 or SA PCIe Port 9 or SA For further details Hub EDS. SATA / PCIe Col Values: SATA, PCIE Port to operate as PCIe Port 10 or SA For further details Hub EDS. SATA / PCIe Col Values: SATA, PCIE Col Values: SATA, PCIE Port 11 or SA PCIE Port 11 or SA PCIE Port 13 or SA For further details Hub EDS. SATA / PCIE Col Values: SATA, PCIE PORT 13 or SA For further details Hub EDS. SATA / PCIE Col Values: SATA, PCIE COL	mbo Port 0 CIe (or GbE), GPIO - Th s either: TA Port 0 (LP) TA Port 0 (H) s on Flex I/O see Skylake mbo Port 1 CIe (or GbE), GPIO - Th s either: TA Port 1 (LP) ATA Port 1 (H) s on Flex I/O see Skylake mbo Port 2 CIe (or GbE), GPIO - Th s either: ATA Port 1 (LP) ATA Port 1 (LP) ATA Port 1 (LP) S on Flex I/O see Skylake mbo Port 3 CIe (or GbE), GPIO - Th s either: ATA Port 2 (LP) ATA Port 2 (LP) ATA Port 1 (H)	his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe H / LP Platform Controller his setting configures the PCIe H / LP Platform Controller	SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-H SKL-S	SATA SATA SATA SATA PCIe (or GbE) GPIO SATA SATA PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) SATA PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) SATA



Table 2-10. Intel[®] FIT - Flex I/O (Sheet 6 of 10)

#		Parameter		Platform	Settings
	SATA / PCIe Combo Port / Values: SATA, PCIe (or Gb port to operate as either: PCIe Port 15 or SATA Port 2	4 E), GPIO - This setting config (H)	jures the PCIe	SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) SATA
	For further details on Flex I/0 Hub EDS.	D see Skylake H / LP Platform	Controller		
	SATA / PCIe Combo Port 5 Values: SATA, PCIe (or GbE), GPIO - This setting configures the PCIe port to operate as either: PCIe Port 16 or SATA Port 3 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS			SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) SATA
	SATA / PCIe Combo Port 6 Values: SATA, PCIe (or GbE), GPIO - This setting configures the PCIe port to operate as either: PCIe Port 17 or SATA Port 4 (H) For further details on Flex I/O see Skylake H / LP Platform Controller			SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) SATA
	SATA / PCIe Combo Port 7 Values: SATA, PCIe (or GbE), GPIO - This setting configures the PCIe port to operate as either: PCIe Port 18 or SATA Port 5 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.		SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) PCIe (or GbE)	
	SATA / PCIe Combo Port 8 Values: SATA, PCIe (or GbE), GPIO - This setting configures the PCIe port to operate as either: PCIe Port 19 or SATA Port 6 (H) For further details on Flex I/O see Skylake H / LP Platform Controller			SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) PCIe (or GbE)
	SATA / PCIe Combo Port 9 Values: SATA, PCIe (or GbE), GPIO - This setting configures the PCIe port to operate as either: PCIe Port 20 or SATA Port 7 (H) For further details on Flex I/O see Skylake H / LP Platform Controller			SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) PCIe (or GbE)
Click or	Flex I/O in the left tabs m	enu> SATA / PCIe Combo	Port Select Po	plarity is expande	d by default:
▼ SA	TA / PCle Combo Port Selec	ct Polarity 5			
	Parameter	Value		Help Text	
Polarity S	Select SATA / PCle Combo Port 0	0 = PCle	This setting is us	sed to determine the na	tive mode con
Polarity S	Select SATA / PCIe Combo Port 1	0 = PCle	This setting is us	sed to determine the na	tive mode con
Polarity \$	Polarity Select SATA / PCle Combo Port 2 0 = PCle		This setting is used to determine the native mode con		
Polarity Select SATA / PCle Combo Port 3 0 = PCle		0 = PCle	This setting is us	sed to determine the na	tive mode con
Polarity \$	Polarity Select SATA / PCle Combo Port 4 0 = SATA		This setting is us	sed to determine the na	tive mode con
Polarity \$	Select SATA / PCle Combo Port 5	0 = SATA	This setting is us	sed to determine the na	tive mode con
Polarity S	Select SATA / PCle Combo Port 6	0 = SATA	This setting is us	sed to determine the na	tive mode con
Polarity S	Select SATA / PCle Combo Port 7	0 = PCle	This setting is us	sed to determine the na	tive mode con



Table 2-10. Intel[®] FIT - Flex I/O (Sheet 7 of 10)

#	Parameter	Platform	Settings
	Flex I/O - SATA / PCI e Combo Port Select Polarity		
	Polarity Select SATA / PCLe Combo Port 0	SKI-Y	SATA
	Values: $0 = SATA/0 = PCLe$ - This setting is used to determine the	SKL-U	SATA
	native mode configuration for SATA / PCIe Combo Port 0.	SKL-H	PCIe
	For further details on Flex I/O see Skylake H / LP Platform Controller	SKL-S	PCIe
	Hub EDS.		DOL
	Volume O SATA (O DCLe. This setting is used to determine the	SKL-Y	PCIe
	native mode configuration for SATA / PCIe Combo Port 1.	SKL-U SKL-H	PCIe
	For further details on Flex I/O see Skylake H / LP Platform Controller	SKL-S	PCIe
	Hub EDS.	O.N.E O	
	Polarity Select SATA / PCIe Combo Port 2	SKL-Y	PCIe
	Values: 0 = SATA/0 = PCIe - This setting is used to determine the	SKL-U	PCIe
	For further details on Flex I/O see Skylake H / LP Platform Controller	SKL-H	PCIe
	Hub EDS.	SKL-S	PCIE
	Polarity Select SATA / PCI e Combo Port 3	SKL-Y	PCIe
	Values: 0 = SATA/0 = PCIe - This setting is used to determine the	SKL-U	PCIe
	native mode configuration for SATA / PCIe Combo Port 3.	SKL-H	PCIe
	For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-S	PCIe
	Polarity Select SATA / PCI e Combo Port 4	SKL-Y	NA
	Values: 0 = SATA/0 = PCIe - This setting is used to determine the	SKL-U	NA
	native mode configuration for SATA / PCTe Combo Port 4.	SKL-H	SATA
	Hub EDS.	SKL-S	PCIe
	Polarity Select SATA / PCIe Combo Port 5	SKL-Y	NA
	Values: 0 = SATA/0 = PCIe - This setting is used to determine the	SKL-U	NA
	hative mode configuration for SATA / PCTe Combo Port 5.	SKL-H	SATA
	Hub EDS.	SKL-S	PCIe
	Polarity Select SATA / PCI e Combo Port 6	SKL-Y	NA
	Values: 0 = SATA/0 = PCIe - This setting is used to determine the	SKL-U	NA
	native mode configuration for SAIA / PCIe Combo Port 6.	SKL-H	SATA
	Hub EDS.	SKL-S	PCIe
	Polarity Select SATA / PCI e Combo Port 7	SKL-Y	NA
	Values: $0 = SATA/0 = PCIe$ - This setting is used to determine the	SKL-U	NA
	Franking mode configuration for SATA / PCIE Compo Port 7.	SKL-H	PCIe
	Hub EDS.	SKL-S	PCIe
	Polarity Select SATA / PCIe Combo Port 8	SKL-Y	NA
	Values: 0 = SATA/0 = PCIe - This setting is used to determine the	SKL-U	NA
	For further details on Elev I/O see Skylake H / LB Platform Controller	SKL-H	PCIe
	Hub EDS.	SKL-S	PCIe
	Polarity Select SATA / PCI e Combo Port 9	SKL-Y	NA
	Values: 0 = SATA/0 = PCIe - This setting is used to determine the	SKL-U	NA
	native mode configuration for SAIA / PCIe Combo Port 9.	SKL-H	PCIe
	Hor Turther details on Flex 1/O see Skylake H / LP Platform Controller Hub EDS.	SKL-S	PCIe
	1	1	

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Table 2-10. Intel[®] FIT - Flex I/O (Sheet 8 of 10)

Click on Flex I/O in the left tabs menu> USB3 Port Configuration is expanded by default:

	Parameter	Value		Help Text		
USB3 /	PCIe Combo Port 0	PCIe (or GbE)	'USB3'-PCIe	Port 1 is statically	assigned to USB3 Port 5, 'PC	
USB3 /	PCIe Combo Port 1	PCIe (or GbE)	'USB3'-PCIe	Ie Port 2 is statically assigned to USB3 Port 6, 'PC		
USB3 /	PCIe Combo Port 2	USB3	'USB3'-PCIe	Port 3 is statically	assigned to USB3 Port 9, 'PC	
USB3 /	PCIe Combo Port 3	PCIe (or GbE)	'USB3'-PCIe	Port 4 is statically	assigned to USB3 Port 10, 'F	
USB3 /	SSIC Combo Port 1	USB3	-			
#	-	Parameter		Platform	Settings	
	Values: PCIe (or GbE), USB3 - This setting configures the PCIe port to operate as either: PCIe Port 1 or USB3 Port 5 (LP) USB3 Port 7 or PCIe Port 1 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS. USB3 / PCIe Combo Port 1 Values: PCIe (or GbE), USB3 - This setting configures the PCIe port to operate as either: PCIe Port 6 or USB3 Port 2 (LP)		orm Controller es the PCIe port	SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S	PCIe (or GbE) USB3 USB3 USB3 USB3 USB3	
	USB3 Port 8 or PCIe P For further details on I Hub EDS.	ort 2 (H) Flex I/O see Skylake H / LP Platfo	orm Controller			
	USB3 / PCIe Combo Port 2 Values: PCIe (or GbE), USB3 - This setting configures the PCIe port to operate as either USB3 Port 9 or PCIe Port 3. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS. USB3 / PCIe Combo Port 3 Values: PCIe (or GbE), USB3 - This setting configures the PCIe port to operate as either USB3 Port 10 or PCIe Port 4. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.		s the PCIe port to er details on Flex	SKL-Y SKL-U SKL-H SKL-S	NA NA USB3 PCIe (or GbE)	
			s the PCIe port to er details on Flex	SKL-Y SKL-U SKL-H SKL-S	NA NA USB3 USB3	
	USB3 / SSIC Combo Values: USB3, SSIC either USB3 or SSIC. Platform Controller Hu	Port 1 - This setting configures USB3 Poi For further details on Flex I/O set b EDS.	rt 1 to operate as ee Skylake H / LP	SKL-Y SKL-U SKL-H	USB3 USB3 USB3	



Table 2-10. Intel[®] FIT - Flex I/O (Sheet 9 of 10)

Click on Flex I/O in the left tabs menu> XHCI Port Configuration is expanded by default:

XHCI Port Configuration

Parameter	Value	Help Text
XHCI Port 1 Ownership	XHCI	This setting configures USB3 Port 1 to operate as either XHCI or
XHCI Port 2 Ownership	XHCI	This setting configures USB3 Port 2 to operate as either XHCI or
XHCI Port 3 Ownership	XHCI	This setting configures USB3 Port 3 to operate as either XHCI or
XHCI Port 4 Ownership	XHCI	This setting configures USB3 Port 4 to operate as either XHCI or
XHCI Port 5 Ownership	Non-XHCI	This setting configures USB3 Port 5 to operate as either XHCI or
XHCI Port 6 Ownership	Non-XHCI	This setting configures USB3 Port 6 to operate as either XHCI or
XHCI Port 7 Ownership	XHCI	This setting configures USB3 Port 7 to operate as either XHCI or
XHCI Port 8 Ownership	XHCI	This setting configures USB3 Port 8 to operate as either XHCI or
XHCI Port 9 Ownership	XHCI	This setting configures USB3 Port 9 to operate as either XHCl or
XHCI Port 10 Ownership	Non-XHCI	This setting configures USB3 Port 10 to operate as either XHCI

#	Parameter	Platform	Settings
	Flex I/O - XHCI Port Configuration		
	VUOL Dant 4 Orangenshin	CKL V	NUCL
	XHCI Port I Ownership	SKL-Y	XHCI
	Values: XHCI, Non-XHCI - This setting configures USB3 Port 1 to	SKL-U	XHCI
	Skylake H / LP Platform Controller Hub EDS	SKL-H	XHCI
		SKL-S	XHCI
	XHCI Port 2 Ownership	SKL-Y	XHCI
	Values: XHCI, Non-XHCI - This setting configures USB3 Port 2 to	SKL-U	XHCI
	operate as either XHCI or Non-XHCI. For further details on Flex I/O see	SKL-H	XHCI
	Skylake H / LP Platform Controller Hub EDS.	SKL-S	XHCI
	XHCI Port 3 Ownership	SKL-Y	XHCI
	Values: XHCI, Non-XHCI - This setting configures USB3 Port 3 to operate as either XHCI or Non-XHCI. For further details on Flex I/O see	SKL-U	XHCI
		SKL-H	XHCI
	Skylake H / LP Platform Controller Hub EDS.	SKL-S	XHCI
	XHCI Port 4 Ownership	SKL-Y	XHCI
	Values: XHCI, Non-XHCI This setting configures USB3 Port 4 to	SKL-U	XHCI
	operate as either XHCI or Non-XHCI. For further details on Flex I/O see	SKL-H	XHCI
	Skylake H / LP Platform Controller Hub EDS.	SKL-S	XHCI
	XHCI Port 5 Ownership	SKL-Y	Non-XHCI
	Values: XHCI, Non-XHCI - This setting configures USB3 Port 5 to	SKL-U	XHCI
	operate as either XHCI or Non-XHCI. For further details on Flex I/O see	SKL-H	Non-XHCI
	Skylake H / LP Platform Controller Hub EDS.	SKL-S	ХНСІ
	XHCI Port 6 Ownership	SKL-Y	Non-XHCI
	Values: XHCI, Non-XHCI - This setting configures USB3 Port 6 to	SKL-U	ХНСІ
	operate as either XHCI or Non-XHCI. For further details on Flex I/O see	SKL-H	Non-XHCI
	Skylake H / LP Platform Controller Hub EDS.	SKL-S	Non-XHCI
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Table 2-10. Intel[®] FIT - Flex I/O (Sheet 10 of 10)

#	Parameter	Platform	Settings
	XHCI Port 7 Ownership	SKL-Y	NA
	Values: XHCI, Non-XHCI - This setting configures USB3 Port 7 to	SKL-U	NA
	operate as either XHCI or Non-XHCI. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-H	XHCI
		SKL-S	XHCI
	XHCI Port 8 Ownership	SKL-Y	NA
	Values: XHCI, Non-XHCI - This setting configures USB3 Port 8 to	SKL-U	NA
	operate as either XHCI or Non-XHCI. For further details on Flex I/O see	SKL-H	XHCI
	Skylake H / LP Platform Controller Hub EDS.	SKL-S	XHCI
	XHCI Port 9 Ownership	SKL-Y	NA
	Values: XHCI, Non-XHCI - This setting configures USB3 Port 9 to	SKL-U	NA
	operate as either XHCI or Non-XHCI. For further details on Flex I/O see	SKL-H	XHCI
	Skylake H / LP Platform Controller Hub EDS.	SKL-S	XHCI
	XHCI Port 10 Ownership	SKL-Y	NA
	Values: XHCI, Non-XHCI - This setting configures USB3 Port 10 to	SKL-U	NA
	operate as either XHCI or Non-XHCI. For further details on Flex I/O see	SKL-H	Non-XHCI
	Skylake H / LP Platform Controller Hub EDS.	SKL-S	Non-XHCI



Table 2-11. Intel[®] FIT - Internal PCH Buses (Sheet 1 of 8)

• OPI Configur	ation	ft tabs menu>	 OPI Configuration is ex 	panded by defaul	t:	
Parameter	Value		Help	Text		
1 Link Speed	GT2	This setting	configures the OPI Link Speed. For furt	her details see Skylake BIO	S Writers Guide.	
I Link Width	8 Lanes	-				
I Link Voltage 0.95 Volts -						
#	Parameter			Platform	Settings	
OPI Lir Values further OPI Lir Values the OPI Values Voltage	al PCH Buses - OPI Co hk Speed : GT2/GT4 - This settir details see Skylake BIO hk Width : 1 Lanes, 2 Lanes, 4 I Link Width. For further hk Voltage : 0.85 Volts, 0.95 Volt . For further details see al PCH Buses in the le iguration 2	nfiguration g configures th S Writers Guide Lanes, 8 Lanes details see Sky s - This setting Skylake BIOS V ft tabs menu>	e OPI Link Speed. For s - This setting configures lake BIOS Writers Guide. configures the OPI Link Writers Guide. • DMI Configuration is ex	SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S SKL-S		
Param	neter	Value		Help Text		
VI Lane Reversa	al No		This setting allows the DM	I Lane signals to be reversed. For furt		
/II RequesterID I	Enabled Yes		This setting is applicable for	or platforms that contain	n multiple proc	
MI Port Staggeri	ng Yes		This setting configures DM	I for Port Staggering. F	or further detail	
ŧ		Parameter		Platform	Settings	
3	Internal PCH B	uses - DMI Co	nfiguration			
DMI La Values reversed EDS.	DMI Lane Reversal Values: Yes/No - This setting allows the DMI Lane signals to be reversed. For further details see Skylake H / LP Platform Controller Hub EDS.			SKL-Y SKL-U SKL-H	No No No	
DMI Re Values multiple Flash th	EDS. DMI RequesterID Enabled Values: Yes/No - This setting is applicable for platforms that contain multiple processor sockets. If multiple processors need to access Serial Flash then this needs to be set to 'Yes'. If platform has only one			SKL-S SKL-Y SKL-U SKL-H SKL-S	NA NA No No	



Table 2-11. Intel[®] FIT - Internal PCH Buses (Sheet 2 of 8)

#		Parameter			Settings	
	DMI Port Stagger	ing		SKL-Y	Yes	
	Values: Yes/No -	This setting configures DMI for	or Port Staggering. For	SKL-U	Yes	
	further details see S	Skylake H / LP Platform Contr	oller Hub EDS.	SKL-H	Yes	
				SKL-S	Yes	
Click on	Internal PCH Buse	es in the left tabs menu> e	SPI Configuration is e	xpanded by defau	ilt:	
▼ eSF	Pl Configuration	3				
	Parameter	Value		Help Text		
eSPI / EC	Boot Enabled	Yes	-			
eSPI / EC	Bus Frequency	60MHz	-			
eSPI / EC	CRC Check Enabled	Yes	-			
eSPI / EC	Max Outstanding R	2	-			
eSPI / EC	Max Read Request	64 bytes	-			
eSPI / EC	Max Read Request	64 bytes	-			
eSPI / EC	Max Read Request	64 bytes	-			
eSPI / EC	Max Virtual Wire Ch	8	-			
eSPI / EC	Maximum I/O Mode	Single, Dual and Quad	-			
eSPI / EC	OOB Channel Enabled	Yes	-			
eSPI / EC	Peripheral Channel	Yes	-			
eSPI / EC	Slave Device Max R	Disabled	-			
eSPI / EC	Slave Device Max O	2	-			
eSPI / EC	Slave Device Max R	64 bytes	-			
eSPI / EC	Slave Device Max R	64 bytes	-			
eSPI / EC	Slave Device OOB	Enabled	-			
eSPI / EC	Slave Device Periph	Enabled	-			
eSPI / EC	Slave Device Virtual	Enabled	-			
eSPI / EC	Slave Device CRC C	Yes	-			
eSPI / EC	Slave Device Maxim	Single	-			
eSPI / EC	Slave Device Bus Fr	20MHz	-			
eSPI / EC	Slave Device Max V	8	-			
eSPI / EC	Slave Device Enabled	Disabled	-			



Table 2-11. Intel[®] FIT - Internal PCH Buses (Sheet 3 of 8)

#	Parameter	Platform	Settings
	Internal PCH Buses - eSPI Configuration		
3			
	eSPI / EC Boot Enabled	SKL-Y	Yes
	Values: Yes/No	SKL-U	Yes
		SKL-H	Yes
		SKL-S	Yes
	eSPI / EC Bus Frequency	SKL-Y	60MHz
	20MHz, 24MHz, 30MHz, 40MHz, 60MHz	SKL-U	60MHZ
		SKL-H	
	aSDL / EC CDC Check Enchlad	SKL-S	No
		SKL-Y	NO
		SKL-U	No
		SKL-S	No
	eSPL / EC Max Outstanding Requests for Master Attached Flash	SKL-V	2
	Channel	SKL-II	2
	Values: 1, 2	SKL-H	2
		SKL-S	2
	eSPL / FC Max Read Request Payload size for Master Attached	SKI-Y	- 64 bytes
	Flash Channel	SKL-U	64 bytes
	Values: 64 bytes, 128 bytes, 256 bytes, 512 bytes, 1024 bytes,	SKL-H	64 bytes
	2048 bytes, 4096 bytes	SKL-S	64 bytes
	eSPL / EC Max Read Request Payload size for OOB Channel	SKL-Y	64 bytes
	Values: 64 bytes, 128 bytes, 256 bytes, 512 bytes, 1024 bytes,	SKL-U	64 bytes
	2048 bytes, 4096 bytes	SKL-H	64 bytes
		SKL-S	64 bytes
	eSPI / EC Max Read Request Payload size for Peripheral Channel	SKL-Y	64 bytes
	Values: 64 bytes, 128 bytes, 256 bytes, 512 bytes, 1024 bytes,	SKL-U	64 bytes
	2048 bytes, 4096 bytes	SKL-H	64 bytes
		SKL-S	64 bytes
	eSPI / EC Max Virtual Wire Channels	SKL-Y	8
	Values: 8, 4, 2, 1	SKL-U	8
		SKL-H	8
		SKL-S	8
	eSPI / EC Maximum I/O Mode	SKL-Y	Single, Dual and Quad
	Values: Single, Single and Dual, Single and Quad, Single Dual and	SKL-U	Single, Dual and Quad
	Quad	SKL-H	Single, Dual and Quad
		SKL-S	Single, Dual and Quad
	eSPI / EC OOB Channel Enabled	SKL-Y	Yes
	Values: Yes/No	SKL-U	Yes
		SKL-H	Yes
	SDL (FC Desighered Channel Enchlad	SKL-S	Yes
		SKL-I	Vos
		SKL-U	Ves
		SKL-II	Ves
	eSPL / FC Slave Device Max Read Dequest OOR Channel Enable	SKL-V	ΝΔ
	Values: Fnabled/Disabled	SKI-U	NA
		SKI-H	Disabled
		SKL-S	Disabled
	eSPL / FC Slave Device Max Outstanding Requests	SKI-Y	NA
	set i / Le olaro Derico hax outstallung requests	SKI-U	NA
		SKL-H	2
		SKL-S	2
L		1	



#	Parameter	Platform	Settings
-	eSPI / EC Slave Device Max Read Request Payload size for OOB	SKL-Y	64 bytes
	Channel	SKL-U	64 bytes
		SKL-H	64 bytes
		SKL-S	64 bytes
	eSPI / EC Slave Device Max Read Request Payload size for	SKL-Y	64 bytes
		SKL-U	64 bytes
		SKL-H	64 bytes
	aSDL / FC Slove Device OOD Channel Fredele	SKL-S	64 Dytes
	Values: Enabled / Disabled	SKL-Y	
	Values. Ellableu/Disableu	SKL-U	Enabled
		SKL-S	Enabled
	eSPL / FC Slave Device Perinheral Channel Enable	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
		SKL-H	Enabled
		SKL-S	Enabled
-	eSPI / EC Slave Device Virtual Wire Channel Enabled	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
		SKL-H	Enabled
		SKL-S	Enabled
	eSPI / EC Slave Device CRC Check Enabled	SKL-Y	NA
	Values: Yes/No	SKL-U	NA
		SKL-H	Yes
		SKL-S	Yes
	eSPI / EC Slave Device Maximum I/O Mode	SKL-Y	NA
		SKL-U	NA
		SKL-H	Single
	oSPL / EC Slave Device Bus Frequency	SKL-S	NA
	esri / Ec slave Device bus riequency	SKL-1	NΔ
		SKL-H	20MHz
		SKL-S	20MHz
-	eSPI / EC Slave Device Max Virtual Wire Channels	SKL-Y	NA
		SKL-U	NA
		SKL-H	8
		SKL-S	8
	eSPI / EC Slave Device Enabled	SKL-Y	NA
	Values: Enabled/Disabled	SKL-U	NA
		SKL-H	Disabled
		SKL-S	Disabled
Click	on Internal PCH Buses in the left tabs menu> PCH Timer Configuration	n is expanded by o	default:
•	PCH Timer Configuration 4		
	Parameter	Va	lue Help
APW	ROK Timing	2 ms	This sof
PCH	clock output stable to PROCPWRGD high (tPCH45)	1 ms	This set
PCIe	Power Stable Timer (tPCH33)	Disabled	This set
PRO	CPWRGD and SYS_PWROK high to SUS_STAT# de-assertion (tPCH46)	1 ms	This set

Table 2-11. Intel[®] FIT - Internal PCH Buses (Sheet 4 of 8)



Table 2-11. Intel[®] FIT - Internal PCH Buses (Sheet 5 of 8)

#	Parameter	Platform	Settings
	Internal PCH Buses - PCH Timer Configuration		
4			
	APWROK Timing	SKL-Y	2 ms
	Values: 2ms, 4ms, 8ms, 16ms - This soft strap determines the time	SKL-U	2 ms
	between the SLP_A# pin de-asserting and the APWROK timer expiration.	SKL-H	2 ms
	FOI TUITINEI GETAIIS SEE SKYIAKE H / LP Platform Controller Hub EDS.	SKL-S	2 ms
	PCH clock output stable to PROCPWRGD high (tPCH45)	SKL-Y	1 ms
	Values: 100ms, 50ms, 5ms, 1ms - This setting configures the	SKL-U	1 ms
	minimum timing from XCK_PLL locked to CPUPWRGD high. For further	^{ner} SKL-H 1 ms	
	details see Skylake H / LP Platform Controller Hub EDS.	SKL-S	1 ms
	PCIe Power Stable Timer (tPCH33)	SKL-Y	Disabled
	Values: Enabled/Disabled - This setting configures the enables /	SKL-U	Disabled
	disables the t36 timer. When enabled PCH will count 99ms from PWROK	SKL-H	Disabled
	setting is "Disabled".	SKL-S	Disabled
	PROCPWRGD and SYS_PWROK high to SUS_STAT# de-assertion	SKL-Y	1 ms
	(tPCH46)	SKL-U	1 ms
	Values: 1ms, 2ms, 5ms - This setting configures the minimum timing	SKL-H	1 ms
	Skylake H / LP Platform Controller Hub EDS.	SKL-S	1 ms



Table 2-11. Intel[®] FIT - Internal PCH Buses (Sheet 6 of 8)

Click on Internal PCH Buses in the left tabs menu> SMBus / SMLink Configuration is expanded by default:

▼ SMBu	s / SMLink Con	figuration 5			
Pa	arameter	Value		Help Te	đ
Intel(R) SMBL	us ASD Address En	No	This setting enables / disa	bles the Intel(R) SMBus	Alert Sending Device. For de
Intel(R) SMBL	us ASD Address	0x00	This setting configures the	e Intel(R) SMBus Alert S	Sending Device Address. For d
Intel(R) SMBu	us I2C Address En	No	This setting enables / disa	bles the Intel(R) SMBus	12C Address. Note: This setti
Intel(R) SMBu	us I2C Address	0x00	This setting configures the	Intel(R) SMBus I2C Ad	dress. Note: This setting is on
Intel(R) SMBu	us MCTP Address	No	This setting enables / disa	bles the Intel(R) SMBus	MCTP Address. Note: This se
Intel(R) SMBu	us MCTP Address	0x00	This setting configures the	Intel(R) SMBus MCTP /	Address. Note: This setting is
Intel(R) SMBu	us Subsystem Ven	0x0000000	This setting configures the	e Intel(R) SMBus Subsy	stern Vendor and Device ID for
SMBus / SML	ink TCO Slave Con	Intel(R) SMBus	This setting configures the	TCO Slave connection	to ether the Intel(R) SMBus or
SMLink0 Enab	bled	Yes	This setting enables / disa	bles SMLink0 interface.	For further details see Skyla
SMLink0 Freq	quency	1 MHz	This setting determines th	e frequency at which th	e SMLink0 will operate. Note:
SMLink1 Enat	bled	Yes	This setting enables / disa	bles SMLink1 interface.	For further details see Skyla
SMLink1 Freq	quency	100 KHz	This setting determines th	e frequency at which th	e SMLink1 will operate. Note:
SMLink1 GP T	Farget Address	0x00	This setting configures SM	4Link1 GP Target Addre	ss. For further details see Sl
SMLink1 GP T	Farget Address En	No	This setting enables / disa	bles SMLink1 GP Target	Address interface. For furthe
SMLink1 12C	Target Address	0x00	This setting configures SM	4Link1 12C Target Addre	ess. For further details see S
SMLink1 I2C	Target Address En	No	This setting enables / disa	bles the SMLink1 I2C T	arget Address . For further de
#		Parameter		Platform	Settings
5	nternal PCH Buse	es - SMBus / SMLink Configu	uration		
In	ntel® SMBus ASD	Address Enable		SKL-Y	No
Va	alues: Yes/No - T	his setting enables / disables t	he Intel® SMBus Alert	SKL-U	No
Se	r further details.	uetalis see Skylake H / LP SPI	rogramming guide	SKL-H	No
1.0	tale SMPue ACD	Address - This setting config	ures the Intel® SMDue	SKL-S	
Ale	ert Sending Device	e Address. For details see Skvl	ake H / LP SPI	SKL-1	0x0000000
Pr	ogramming guide	for further details.		SKI-H	0x00000000
				SKL-S	0x00000000



Table 2-11. Intel[®] FIT - Internal PCH Buses (Sheet 7 of 8)

#	Parameter	Platform	Settings
	Intel® SMBus I2C Address Enabled	SKL-Y	No
	Values: Yes/No - This setting enables / disables the Intel® SMBus I2C	SKL-U	No
	Address. Note: This setting is only used for testing purposes. The	SKL-H	No
	recommended setting is no .	SKL-S	No
	Intel® SMBus I2C Address - This setting configures the Intel® SMBus	SKL-Y	0x0000000
	I2C Address. Note: This setting is only used for testing purposes. The	SKL-U	0x0000000
	recommended setting is 0000000 .	SKL-H	0x0000000
		SKL-S	0x0000000
	Intel® SMBus MCTP Address Enabled	SKL-Y	No
	Values: Yes/No - This setting enables / disables the Intel® SMBus	SKL-U	No
	MCTP Address. Note: This setting is only used for testing purposes. The	SKL-H	No
	recommended setting is no .	SKL-S	No
	Intel® SMBus MTCP Address - This setting configures the Intel®	SKL-Y	0x0000000
	SMBus MCTP Address. Note: This setting is only used for testing	SKL-U	0x0000000
	purposes. The default setting is 0000000 .	SKL-H	0x0000000
		SKL-S	0x0000000
	Intel® SMBus Subsystem Vendor & Device ID for ASF - This setting	SKL-Y	0x0000000
	contigures the Intel® SMBus Subsystem Vendor & Device ID for ASF. For	SKL-U	0x0000000
	details see Skylake H / LP SPI Programming guide further details.	SKL-H	0x0000000
		SKL-S	0x0000000
	SMBus / SMLink TCO Slave Connection	SKL-Y	Intel [®] SMBus
	Values: Intel® SMBus, SMLinkO - This setting configures the TCO	SKL-U	Intel® SMBus
	Slave connection to ether the Intel® SMBus or SMLinkO. For further	SKL-H	Intel [®] SMBus
	details see Skylake H / LP Plation III Controller Hub EDS.	SKL-S	Intel® SMBus
	SMLink0 Enabled	SKL-Y	Yes
	Values: Yes/No - This setting enables / disables SMLink0 interface. For	SKL-U	Yes
	further details see Skylake H / LP Platform Controller Hub EDS. Note: If	SKL-H	Yes
		SKL-S	Yes
	SMLinkO Frequency	SKL-Y	1 MHz
	Values: 100KHz, 400KHz, 1 MHz - This setting determines the	SKL-U	1 MHz
	setting is "1MHz"	SKL-H	1 MHz
		SKL-S	1 MHz
	SMLink1 Enabled	SKL-Y	Yes
	Values: Yes/No - This setting enables / disables SMLink1 interface. For	SKL-U	Yes
	Turiner details see Skylake H / LP Platform Controller Hub EDS. Note: This setting must be set to "Ves" if using PCH / MCP Thermal reporting	SKL-H	Yes
		SKL-S	Yes
	SMLink1 Frequency	SKL-Y	100 KHz
	Values: 100KHz, 400KHz, 1 MHz - This setting determines the	SKL-U	100 KHz
	setting is "100KHz"	SKL-H	100 KHz
		SKL-S	100 KHz
	SMLink1 GP Target Address - This setting configures SMLink1 GP	SKL-Y	0x0000000
	Hub EDS	SKL-U	0x0000000
		SKL-H	0x0000000
		SKL-S	0x00000000
	SMLink1 GP Target Address Enabled	SKL-Y	No
	Values: Yes/No - This setting enables / disables SMLink1 GP Target	SKL-U	No
	Controller Hub EDS. Note: This setting must be set to "Yes" if using PCH	SKL-H	No
	/ MCP Thermal reporting.	SKL-S	NO
	SMLink1 I2C Target Address - This setting configures SMLink1 I2C	SKL-Y	0x0000000
	Target Address. For further details see Skylake H / LP Platform Controller	SKL-U	0x0000000
		SKL-H	0x0000000
		SKL-S	0x0000000



Table 2-11. Intel[®] FIT - Internal PCH Buses (Sheet 8 of 8)

#	Parameter	Platform	Settings
	SMLink1 I2C Target Address Enabled	SKL-Y	No
	Values: Yes/No - This setting configures SMLink1 I2C Target Address.	SKL-U	No
	For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-H	No
		SKL-S	No



Table 2-12. Intel[®] FIT - GPIO (Sheet 1 of 2)

LAN / GPIO Select	1			
Parameter	Value		Help Text	
I PHY Power Control GPD1 LANP	НҮРС	-	-	
ŧ	Parameter		Platform	Settings
GPIO - LAN / GPIO Sel	ect			
LAN PHY Power Control GPD11 Signal Configuration			SKL-Y SKL-U SKL-H SKL-S	LANPHYPC LANPHYPC LANPHYPC LANPHYPC
WLAN / GPIO Select Parameter	2 Value		Help Text	
WLAN# / GPD9 Signal C SLP	WLAN#	-		
	Parameter		Platform	Settings
SLP_WLAN# / GPD9 S	ignal Configuratior		SKL-Y SKL-U SKL-H	SLP_WLAN# SLP_WLAN# SLP_WLAN#
k on GPIO in the left tabs m	enu> Platform Po	ver / GPIO is expan	ded by default:	SLP_WLAN#
Platform Power / G	PIO 3	10	U	ala Tavt
P A# / GPD6 Signal Configur	SIP A#	-	n	eip Text
P_S3# / GPD4 Signal Configu	. SLP_S3#	-		
P_S4# / GPD5 Signal Configu	. SLP_S4#	-		
P_S5# / GPD10 Signal Config	. SLP_S5#	-		
t	Parameter		Platform	Settings
GPIO - Platform Power	/ GPIO			



#		Parameter		Platform	Settings	
	SLP_A# / GPD6 Sig	nal Configuration		SKL-Y	SLP_A#	
				SKL-U	SLP_A#	
				SKL-H	SLP_A#	
				SKL-S	SLP_A#	
	SLP_S3# / GPD4 Si	gnal Configuration		SKL-Y	SLP_S3#	
				SKL-U	SLP_S3#	
				SKL-H	SLP_S3#	
				SKL-S	SLP_S3#	
	SLP_S4# / GPD5 Si	gnal Configuration		SKL-Y	SLP_S4#	
				SKL-U	SLP_S4#	
				SKL-H	SLP_S4#	
				SKL-S	SLP_S4#	
	SLP_S5# / GPD10 9	Signal Configuration		SKL-Y	SLP_S5#	
				SKL-U	SLP_S5#	
				SKL-H	SLP_S5#	
				SKL-S	SLP_S5#	
Click or	n GPIO in the left tab	s menu> ME Feature Pins is e	expanded by default	:		
	Parameter	Value		He	lp Text	
NFC Re	set GPIO Select	None	NFC must be	enabled in the Ne	tworking & Connectivity s	
NFC IR	Q GPIO Select	None	NFC must be	NFC must be enabled in the Networking & Connectivity s		
NFC DF	U GPIO Select	None	NFC must be	enabled in the Ne	tworking & Connectivity s	
#	•	Parameter		Platform	Settings	
4	NFC Reset GPIO Sel NFC must be enabled configure this setting. NFC IRQ GPIO Sele NFC must be enabled configure this setting. NFC DFU GPIO Sele NFC must be enabled	lect in the Networking and Connectiv ct in the Networking and Connectiv ct in the Networking and Connectiv	vity section to vity section to vity section to			
	configure this setting.	5	2			

Table 2-12. Intel[®] FIT - GPIO (Sheet 2 of 2)



Table 2-13. Intel[®] FIT - Power (Sheet 1 of 2)

Click or	n Power in the left Platform Powe	tabs m	enu> Platform Power is	expanded by default:			
	Parameter		Value		Help Text		
SLP_A	# / GPD6 Signal Con	figur	SLP_A#	This setting allows	the user to assi	ign the SLP_A# Pow	
SLP_S3	3# / GPD4 Signal Co	nfigu	SLP_S3#	This setting allows	the user to assi	ign the SLP_S3# Pov	
SLP_S4	1# / GPD5 Signal Co	nfigu	SLP_S4#	This setting allows	the user to assi	ign the SLP_S4# Pov	
SLP_S	5# / GPD10 Signal O	onfig	SLP_S5#	This setting allows	the user to assi	ign the SLP_S5# Pov	
#			Parameter		Platform	Settings	
0			Power - Platform Power				
lick or	SLP_A# / GPD6 Signal Configuration Values: SLP_A#, GPD6 - This setting allows the customer to assign the SLP_A# Power Control signal as SLP_A# or as GDP6. For further details see Skylake H / LP Platform Controller Hub EDS. SLP_S3# / GPD4 Signal Configuration Values: SLP_S3#, GPD4 - This setting allows the customer to assign the SLP_S3# Power Control signal as SLP_S3# or as GDP4. For further details see Skylake H / LP Platform Controller Hub EDS. SLP_S4# / GPD5 Signal Configuration Values: SLP_S4#, GPD5 - This setting allows the customer to assign the SLP_S4# Power Control signal as SLP_S4# or as GDP5. For further details see Skylake H / LP Platform Controller Hub EDS. SLP_S4# Power Control signal as SLP_S4# or as GDP5. For further details see Skylake H / LP Platform Controller Hub EDS. SLP_S5# / GPD10 Signal Configuration Values: SLP_S5#, GPD10 - This setting allows the customer to assign the SLP_S5# Power Control signal as SLP_S5# or as GDP10. For further details see Skylake H / LP Platform Controller Hub EDS. SDP_S5# Power Control signal as SLP_S5# or as GDP10. For further details see Skylake H / LP Platform Controller Hub EDS. SDP_S5# Power Configuration Values: SLP_S5# Nemuer Control signal as SLP_S5# or as GDP10. For further details see Skyla				SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S SKL-Y SKL-U SKL-H SKL-S ed by default:	SLP_A# SLP_A# SLP_S3# SLP_S3# SLP_S3# SLP_S3# SLP_S4# SLP_S4# SLP_S4# SLP_S4# SLP_S5# SLP_S5# SLP_S5#	
	Parameter	Val	ue	Help Text			
M3 Powe	r Rail Available Yes						
#			Parameter		Platform	Settings	
2	1	Power -	Intel® ME Power Config	uration			
	M3 Power Rail A Values: Yes/No the firmware. Not Intel® vPro™ plat	vailable - This se e: Suppo form this	tting enables / disables sup ort for M3 is dependent on H s setting must be set to "Ye	port for M3 operation of HW board design. For s".	SKL-Y SKL-U SKL-H	Yes Yes Yes	



Table 2-13. Intel[®] FIT - Power (Sheet 2 of 2)

Click or	n Power in the left	tabs menu> Deep Sx is	expanded by default:			
▼ De	ep Sx	3				
	Parameter	Value	Help Te	ext		
Deep Sx	Enabled	Yes	This requires the target platform to supp	port Deep SX state		
#		Parameter	r	Platform	Settings	
3	Power - Deep Sx					
	Deep Sx Enabled			SKL-Y	Yes	
	Values: Yes/ No	- This setting enables / dis	ables support for Deep Sx	SKL-U	Yes	
	Note: Support for	Deep Sx is board design d	ependent.	SKL-H SKL-S	Yes Yes	



Table 2-14. Intel[®] FIT - Integrated Sensor Hub (Sheet 1 of 2)

Integrated Sensor Hub	Click on Integrated Sensor Hub in the left tabs menu> Integrated Sensor Hub is expanded by default:					by default:
Integrated Sensor Hub Value Help Text Integrated Sensor Hub Signing, OEM/rel - - Integrated Sensor Hub Signing, OEM/rel - - Integrated Sensor Hub Supported - - Integrated Sensor Hub Supported SKL-Y SKL-Y Values: Yes/No SKL-Y SKL-U This setting allows customers to disable ISH on the platform. SKL-Y Values: Tes/No SKL-Y SKL-Y SKL-Y Values: Enabled/Disabled SKL-Y Field is enabled for celling if "Integrated Sensor Hub Supported" field SKL-Y Values: Enabled/Disabled SKL-Y SKL-Y SKL-U This setting determines ISH signing Will be checked against the Intel SKL-H provisioned on the platform. SKL-H SkL-B SkL-Y Values: CEM/Intel, OEM SkL-H provisioned on the platform. SkL-H Parameter Value Values: OEM Parameter Values: CEM/Intel, OEM SkL-H provisioned on the platform. SkL-H provisioned on the platform. SkL	- Intern		-			
Parameter Value Help Toxt ttegrated Sensor Hub Supported - - # Parameter Platform Settings # Integrated Sensor Hub Supported SkL Y SkL V Values: Kes/No SkL V SkL H SkL H This setting allows customers to disable ISH on the platform. SkL H SkL H above is set to "ves". This setting allows customers to disable Sk L H SkL H SkL H above is set to "ves". This setting allows customers to disable Sk L H SkL H SkL H setting determine the base image or OEM public key hash prove up state for ISH. SkL H SkL H Tetegrated Sensor Hub Signing Policy SkL H SkL H SkL H values: CEM/Intel, OEM Fat arge to fat arge in plate) SkL H SkL H Integrated Sensor Hub In the left tabs menu> ISH singe of the ISH code patton including reserved space. It is recommended to be at leas. SkL H	 Integ 	rated Sensor Hu	ID 🚺			
Integrated Sensor Hub Supported Nu - # Parameter Platform SKL-Y SKL-Y Values: For Sensor Hub Integrated Sensor Hub Supported SKL-Y Values: Values: Nub Content of State Values: For Sensor Hub Integrated Sensor Hub Dever Up State SKL-Y Values: For Sensor Hub Supported Values: SKL-Y Values: For Sensor Hub Supported Values: SKL-Y Values: For Sensor Hub Supported SKL-Y SKL-H SKL-Y SKL-U SKL-S SKL-Y Values: For Sensor Hub Supported Totagrated Sensor Hub Signing will be checked against the Intel SKL-B SKL-Y SKL-Y Values: Ce Integrated Sensor Hub In the left tabs menu> 1SH Image is expanded by default: ISH Image Path to you ISH fimmare biary file Parameter Value Path to you	P	arameter	Value	He	elp Text	
Integrated Sensor Hub Signing OEMinal - # Parameter Platform Settings # Integrated Sensor Hub Supported Values: Yes/No SKL-Y SKL-Y This setting allows customers to disable ISH on the platform. SKL-Y SKL-Y SKL-Y SKL-Y SKL-Y Values: Yes/No SKL-Y SKL-Y Field is enabled / Disabled SKL-Y SKL-H SKL-S SKL-Y SKL-Y Values: Enabled/Disabled SKL-Y SKL-H power is set to 'Yes'. This setting allows customers to determine the power up state for IsH. SKL-H Values: CM/Intel, OEM SKL-U SKL-U Values: CM/Intel, OEM SKL-U SKL-U This setting determines ISH signing will be checked against the Intel provisioned and included in the base image or OEM public key hash provisioned and included in the base image or OEM public key hash provisioned and included in the base image or OEM public key hash provisioned and thoused in the set or Yes'. SKL-W SKLew SKL SKL-Y SKL-Y Value Parameter Platform SKL-Y Value Parameter Platform Settings # Parameter </td <td>Integrated S</td> <td>ensor Hub Supported</td> <td>No</td> <td>-</td> <td></td> <td></td>	Integrated S	ensor Hub Supported	No	-		
Integrated Sensor Hub Signing OEMIntel # Parameter Platform Settings Integrated Sensor Hub Supported SKL-Y Values: Yes/No SKL-Y SKL-Y This setting allows customers to disable ISH on the platform. SKL-Y SKL-S SKL-Y Values: Enabled/Obisabled SKL-Y Field is enabled/roling if Integrated Sensor Hub Supported field above is set to 'Yes'. This setting allows customers to determine the power up state for ISH. Values: CoM/Intel, OEM SKL-V Values: CoM/Intel, OEM SKL-U Struey up state for ISH. SKL-U Values: CoM/Intel, OEM SKL-U Values: CoM/Intel, OEM SKL-U Struey visioned and included in the base image or OEM public key hash provisioned and included in the base image or OEM public key hash provisioned and included in the base image or OEM public key hash provisioned and included in the base image or OEM public key hash provisioned and included in the base image or OEM public key hash is StL-U StL-U StHinge Q Parameter Value Parameter Value Parameter Platform StL StL-W StL StL-W StL StL This setting allow so of the ISH code partition including reserved space. It is recommended to be at least 256k	Integrated S	Integrated Sensor Hub Initial P Disabled		-		
# Parameter Platform Settings 1 Integrated Sensor Hub SKL-Y SKL-Y SKL-Y Values: Yes/No This setting allows customers to disable ISH on the platform. SKL-H SKL-H This setting allows customers to disable ISH on the platform. SKL-H SKL-Y Values: Pabled/Disabled SKL-Y SKL-Y Values: Enabled/Disabled SKL-Y SKL-Y Values: Enabled/Disabled SKL-Y SKL-Y Values: CoBM/Intel, OEM SKL-S SKL-H Thisgrated Sensor Hub Signing Policy SKL-H SKL-S Values: CoBM/Intel, OEM SKL-Y SKL-H Tritegrated Sensor Hub is a linging will be checked against the Intel Provisioned on the platform. SKL-H Still addet in the left tabs menu> ISH Image is expanded by default: * * ISH Image 2 Parameter Value Help Text Integrated Sensor Hub - ISH Image Settings # Parameter Platform Settings Ted size (in bytes) of the ISH code partition including reserved space. It is recommended to be at least. particle Path to your ISH firmware binary file SkL-	Integrated S	ensor Hub Sianina	OEM/Intel			
** Parameter Platform Settings Integrated Sensor Hub Integrated Sensor Hub Supported SKL-Y SKL-Y Values: Yes/No SKL-U SKL-H SKL-H This setting allows customers to disable ISH on the platform. SKL-H SKL-H Integrated Sensor Hub Power Up State SKL-Y SKL-Y Values: Enabled/Disabled SKL-Y SKL-Y Field is enabled for editing if "Integrated Sensor Hub Supported" field above is set to 'Yes'. This setting allows customers to determine the power up state for ISH. SKL-Y Values: OEM/Intel, OEM SKL-H SKL-H This setting determines ISH signing will be checked against the Intel provisioned not he platform. SKL-H Still above is set to 'Yes'. This setting allows customers to ISH Image is expanded by default: * * ISH Image Q Parameter Value Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at less # Parameter Platform Settings # Parameter Platform Settings # Integrated Sensor Hub - ISH Image SKL-Y Path to your ISH firmware binary f		1	Demo		Distinguis	
Integrated Sensor Hub Supported Values: Yes /No SKL.Y This setting allows customers to disable ISH on the platform. SKL.H SKL.V SKL.U This setting allows customers to disable ISH on the platform. SKL.H SKL.V SKL.U Values: trabled /Disabled SKL.U Field is enabled for editing if "Integrated Sensor Hub Supported" field above is set to "vest. This setting allows customers to determine the power up state for ISH. SKL.V Values: OEM/Initel, OEM SKL.U This setting determines ISH signing will be checked against the Intel set.Set.U SKL.V Values: OEM/Initel, OEM SKL.U This setting determines ISH signing will be checked against the Intel set.Set.U SKL.U Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: * ISH Image Q Value Parameter Platform Settings Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image Image is expanded by our ISH immare binary file Path to your ISH firmware binary file Path to your ISH firmware binary file Integrated Sensor Hub - ISH code partition including reserved space. It is recommended to be at least 256kb. SKL-Y	#	Integrated	Sensor Hub	ieter	Platform	Settings
Integrated Sensor Hub Supported Values: Yes/No SKL-Y SKL-U This setting allows customers to disable ISH on the platform. SKL-Y SKL-U Values: Inabled/Disabled Field is enabled for editing if "Integrated Sensor Hub Supported" field above is set to "yes". This setting allows customers to determine the power up state for ISH. SKL-Y SKL-U Values: CoEVIntel, OEM Values: COEVIntel, OEM SKL-V SKL-U This setting determines ISH signing Policy Values: OEVIntel, OEM SKL-V SKL-U This setting determines ISH signing will be checked against the Intel provisioned hash included in the base image or OEM public key hash provisioned an the platform. SKL-H SKL-B Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: * ISH Image 2 Parameter Value Value Path to your ISH fimware binary file. * Parameter Platform Settings Integrated Sensor Hub - ISH code partition including reserved space. It is recommended to be at leas * Integrated Sensor Hub - ISH image SkL-Y SkL-Y Integrated Sensor Hub - ISH code partition including reserved space. It is recommended to be at least 256kb. SkL-Y SkL-U Input File SkL-Y SkL-U Path to your ISH firmware binary file		megrateu	Sensor Hub			
Integrated Sensor Hub Supported Values: Yes/No SKL-Y This setting allows customers to disable ISH on the platform. SKL-U SKL-S Integrated Sensor Hub Power Up State SKL-S SKL-Y Values: Enabled/Disabled SKL-V Field is enabled for editing if "Integrated Sensor Hub Supported" field above is set to "Yes". This setting allows customers to determine the power up state for 1SH. SKL-H Integrated Sensor Hub Signing Policy Values: OEM/Intel, OEM SKL-V This setting determines ISH signing will be checked against the Intel provisioned hash included in the base image or OEM public key hash provisioned an the platform. SKL-H Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: SKL-S Value Help Text Mathematical Sensor Hub in the left tabs menu> ISH Image is expanded by default: * ISH Image Q Integrated Sensor Hub - ISH image Integrated Sensor Hub - ISH Image # Parameter Platform Settings Integrated Sensor Hub - ISH Image # Parameter Platform 2 Integrated Sensor Hub - ISH Image # Parameter Platform SKL-Y SkL-W Integrated Sensor Hub - ISH Image SkL-W Integrated Sensor Hub - ISH Image SkL-W Input File SkL Input						
Values: Yes/No SKL-U SKL-U This setting allows customers to disable ISH on the platform. SKL-U SKL-H Integrated Sensor Hub Power Up State SKL-V SKL-U Values: Enabled/Disabled SKL-U SKL-U Field is enabled for oditing if "Integrated Sensor Hub Supported" field above is set to "Yes". This setting allows customers to determine the power up state for ISH. SKL-U Integrated Sensor Hub Signing Policy SKL-U Values: OEM/Intel, OEM SKL-U This setting determines ISH signing will be checked against the Intel provisioned hash included in the base image or OEM public key hash provisioned hash included in the base image or OEM public key hash provisioned on the platform. SKL-U Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: IsH Image 2 Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image # Parameter Platform Settings # Parameter Platform Settings Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image Platform Settings # Parameter Platform Settings Plath to your ISH firmware binary file	Integrated Sensor Hub Support		Sensor Hub Support	ed	SKL-Y	
This setting allows customers to disable ISH on the platform. SKL-H SKL-H Integrated Sensor Hub Power Up State SKL-Y SKL-U Field is enabled /Disabled SKL-U SKL-H Pried is enabled for editing if "Integrated Sensor Hub Supported" field above is set to 'Yes'. This setting allows customers to determine the power up state for ISH. SKL-H Integrated Sensor Hub Signing Policy SKL-Y Values: OEM/Intel, OEM SKL-V This setting determines ISH signing will be checked against the Intel provisioned nath included in the base image or OEM public key hash provisioned on the platform. SKL-H Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: This setting determines ISH signing will be checked against the Intel IsH Image O Parameter Value Help Text Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: * ISH Image O Value Path to your ISH firmware binay file. * Parameter Platform Settings Integrated Sensor Hub - ISH Image * Parameter Platform Settings Integrated Sensor Hub - ISH Image * Parameter Platform Settings Integrated Sensor Hub - ISH code partition including reserved space. It is recommended to be at least 256kb. SKL-Y		Values: Yes/No			SKL-U	
SKL-S SKL-S Values: Enabled/Disabled SKL-Y Field is enabled for editing if 'Integrated Sensor Hub Supported' field above is set to 'Yes''. This setting allows customers to determine the power up state for ISH. SKL-Y Integrated Sensor Hub Signing Policy SKL-U Values: OEM/Intel, OEM SKL-U This setting determines ISH signing will be checked against the Intel provisioned hash included in the base image or OEM public key hash provisioned hash included in the base image or OEM public key hash provisioned on the platform. SKL-U Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: ISH Image 2 Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image # Parameter Platform Settings Integrated Sensor Hub - ISH Image # Parameter Platform Value Integrated Sensor Hub - ISH Image # Parameter Platform Y Integrated Sensor Hub - ISH Image SKL-Y Path to your ISH firmware binary file Integrated Sensor Hub - ISH Image # Parameter Platform SKL-U SKL-U SkL-U Integrated Sensor Hub - ISH Image SKL-Y Path to your ISH firmware binary file SKL-U <td colspan="2">This setting allows customers to disa</td> <td>allows customers to dis</td> <td>able ISH on the platform.</td> <td>SKL-H</td> <td></td>	This setting allows customers to disa		allows customers to dis	able ISH on the platform.	SKL-H	
Integrated Sensor Hub Power Up State SKL-V Values: Enabled /Disabled SKL-U Field is enabled for editing if "Integrated Sensor Hub Supported" field above is set to "Yes". This setting allows customers to determine the power up state for ISH. SKL-H Integrated Sensor Hub Signing Policy SKL-V Values: CDEM/Intel, OEM SKL-U This setting determines ISH signing will be checked against the Intel provisioned on the platform. SKL-H SKL-I SKL-U Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: * ISH Image @ Parameter Value Value Total size (in bytes) of the ISH code partition including resend space. It is recommended to be at leas hpdFile Pat or your ISH firmware binary file. # Parameter Platform Settings Integrated Sensor Hub - ISH code partition including reserved space. It is recommended to be at leas hpdFile Pat to your ISH firmware binary file.					SKL-S	
Values: Enabled / Disabled SKL-U Field is enabled for editing if "Integrated Sensor Hub Supported" field above is set to "Yes". This setting allows customers to determine the power up state for ISH. SKL-H Integrated Sensor Hub Signing Policy SKL-V Values: OEM/Intel, OEM SKL-U This setting determines ISH signing will be checked against the Intel provisioned hash included in the base image or OEM public key hash skL-S SKL-V Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: SKL-V * ISH Image 2 Parameter Value to be at leas hpdFile Path to your ISH firmware binay file. * Parameter Platform # Parameter	Integrated Sensor Hub Power Up			p State	SKL-Y	
Field is enabled for editing if "Integrated Sensor Hub Supported" field bowe is set to 'Yes'. This setting allows customers to determine the power up state for ISH. SKL-Y Integrated Sensor Hub Signing Policy Values: OEM/Intel, OEM This setting determines ISH signing will be checked against the Intel provisioned hash included in the base image or OEM public key hash provisioned hash included in the base image or OEM public key hash skL-S SKL-H SKL-B Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: * * ISH Image 2 Parameter Value Parameter Value Parameter Value Parameter Parameter Parameter Parameter Parameter Platform Settings Integrated Sensor Hub - ISH Image # Parameter Parameter Platform Settings Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH image Integrated Sensor Hub - ISH code partition including reserved space. It is recommended to be at least 256kb. Input File SKL-Y SKL-U SKL-U SKL-H Path to your ISH firmware binary file SKL-H Path to your ISH firmware binary file SKL-H	Values: Enabled/Disabled				SKL-U	
abover up start to Test. This setting allows customers to determine the power up start for TSH. SKL-S Integrated Sensor Hub Signing Policy Values: OEM/Intel, OEM This setting determines TSH signing will be checked against the Intel provisioned hash included in the base image or OEM public key hash provisioned on the platform. SKL-Y SKL-U SKL-H Click on Integrated Sensor Hub in the left tabs menu> TSH Image is expanded by default: Image * ISH Image 2 Parameter Value Mathematication Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at least. # Parameter Parameter Platform Settings Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image Start Parameter Platform Settings Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image SKL-Y Path to your ISH firmware binary file Input File SKL-Y Path to your ISH firmware binary file	Field is enabled for editing if "Integra above is set to "Ves". This setting all			rated Sensor Hub Supported" field	SKL-H	
Integrated Sensor Hub Signing Policy Values: OEM/Intel, OEM This setting determines ISH signing will be checked against the Intel provisioned and his hickleded in the base image or OEM public key hash provisioned on the platform. SKL-Y SKL-U SKL-H SKL-S Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: Image ISH Image 2 Parameter Value Parameter Value Path to your ISH firmware binary file. # Parameter Path to your ISH Image # Parameter Path to your ISH firmware binary file. # Parameter Path to your ISH firmware binary file. # Parameter Path to your ISH firmware binary file. # Parameter Path to your ISH firmware binary file # Parameter Path to your ISH firmware binary file Path to your IS	power up state for ISH.				SKL-S	
Values: OEM/Intel, OEM SKL-U SKL-U This setting determines ISH signing will be checked against the Intel provisioned on the platform. SKL-H SKL-H Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: ISH Image Image * ISH Image 2 Parameter Value Help Text Length 0x40000 Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at leas Input File Patameter Platform Settings # Parameter Platform Settings Integrated Sensor Hub - ISH Image Image Image Image Integrated Sensor Hub - ISH code partition including reserved space. It is recommended to be at least 256kb. SKL-Y Path to your ISH firmware binary file Input File Image SKL-U SKL-U SKL-U Dinary file Input File Image SKL-H <	Integrated Sensor Hub Signing F Values: OEM/Intel, OEM			Policy	SKL-Y	
This setting determines ISH signing will be checked against the Intel provisioned hash included in the base image or OEM public key hash provisioned on the platform. SKL-H SkL-S Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: ISH Image ISH Image Output to the integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: ISH Image Parameter Value				-	SKL-U	
provisioned hash included in the base image or OEM public key hash provisioned on the platform. SKL-S Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: ISH Image 2 Parameter Value Help Text Length 0x40000 Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at leas hputFile Parameter Platform Settings # Parameter Platform Value Parameter Platform Value Parameter Platform Settings Integrated Sensor Hub - ISH Image Platform Settings Integrated Sensor Hub - ISH Image Platform Settings SKL-Y Path to your ISH firmware binary file Input File SKL-Y Path to your ISH firmware binary file SKL-U SKL-H Path to your ISH firmware binary file Path to your ISH firmware binary file Path to your ISH firmware binary file Duty File SKL-H Path to your ISH firmware binary file		This setting	determines ISH signing	will be checked against the Intel	SKL-H	
Provide on the production. Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default: ISH Image Q Parameter Value Help Text Length 0x40000 Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at leas ImputFile Parameter Platform Settings # Parameter Platform Settings # Parameter Platform Settings Q Integrated Sensor Hub - ISH Image Platform Settings Integrated Sensor Hub - ISH Image Platform Settings Input File Input File Plath to your ISH firmware binary file. Input File SKL-U Path to your ISH firmware binary file Input File SKL-U Path to your ISH firmware binary file Bath to your ISH firmware binary file Path to your ISH firmware binary file Bath to your ISH firmware binary file Path to your ISH firmware binary file Bath to your ISH firmware binary file Path to your ISH firmware binary file		provisioned I	hash included in the ba	se image or OEM public key hash	SKL-S	
ISH Image 2 Parameter Value Help Text Length 0x40000 Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at leas InputFile Path to your ISH firmware binary file. # Parameter Platform Settings Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image Path to your ISH firmware binary file. Length - Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at least 256kb. SKL-Y Path to your ISH firmware binary file Input File SKL-U SKL-H Path to your ISH firmware binary file Dath to your ISH firmware binary file	Click or	n Integrated	Sensor Hub in the le	ft tabs menu> ISH Image is ex	panded by default:	
ISH Image 2 Parameter Value Help Text Length 0x40000 Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at leas InputFile Path to your ISH firmware binary file. # Parameter Platform Settings # Parameter Platform Settings Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image Path to your ISH firmware binary file Input File SKL-Y Path to your ISH firmware binary file SKL-Y Path to your ISH firmware binary file SKL-U SKL-H Path to your ISH firmware binary file SKL-H Path to your ISH firmware binary file					·	
Parameter Value Help Text InputFile 0x40000 Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at leas # Parameter Platform Settings Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image SKL-Y Path to your ISH firmware binary file Input File SKL-Y Path to your ISH firmware binary file SKL-U SKL-H Path to your ISH firmware binary file	▼ ISH In	nage	2			
Parameter Ox40000 Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at leas # Parameter Platform Settings # Parameter Platform Settings Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image Platform Settings Integrated sensor Hub - ISH Image SKL-Y Path to your ISH firmware binary file Input File SKL-Y Path to your ISH firmware binary file SKL-U SKL-U Path to your ISH firmware binary file SKL-H SKL-H Path to your ISH firmware binary file	Dr	aramator	Value	Ца	In Taxt	
InputFile Path to your ISH firmware binary file. # Parameter Platform Settings Integrated Sensor Hub - ISH Image Length - Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at least 256kb. SKL-Y Path to your ISH firmware binary file Input File SKL-U SKL-U Path to your ISH firmware binary file SKL-H Path to your ISH firmware binary file	Leasth		Value	Table in (a base) state (CH and a settion include	ip iext	and date by at large
Path to your ISH firmware binary file. # Parameter Platform Settings 2 Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image 2 Length - Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at least 256kb. Input File SKL-Y Input File SKL-U SKL-U Path to your ISH firmware binary file SKL-H Path to your ISH firmware binary file Bina	Length		0X40000	Iotal size (in bytes) of the ISH code partition includ	ling reserved space. It is recomm	nended to be at leas
# Parameter Platform Settings Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image	InputFile			Path to your ISH firmware binary file.		
Integrated Sensor Hub - ISH Image Integrated Sensor Hub - ISH Image Length - Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at least 256kb. Path to your ISH firmware binary file Input File SKL-Y Path to your ISH firmware binary file SKL-H SKL-H Path to your ISH firmware binary file	#		Paran	neter	Platform	Settings
2 Length - Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at least 256kb. File Path to your ISH firmware binary file Input File SKL-Y Path to your ISH firmware binary file SKL-U SKL-U Path to your ISH firmware binary file SKL-H SKL-H Path to your ISH firmware binary file		Integrated	Sensor Hub - ISH Im	nage		
Length - Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at least 256kb. Path to your ISH firmware binary file Input File SKL-Y Path to your ISH firmware binary file SKL-U SKL-U Path to your ISH firmware binary file SKL-H SKL-H Dath to your ISH firmware binary file						
Length - Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at least 256kb. Path to your ISH firmware binary file Input File SKL-V Path to your ISH firmware binary file SKL-U SKL-U Path to your ISH firmware binary file SKL-H SKL-H Path to your ISH firmware binary file	9					
Input File SKL-Y Path to your ISH firmware binary file SKL-U SKL-U Path to your ISH firmware binary file SKL-H Path to your ISH firmware binary file		Length - Tot	tal size (in bytes) of the	e ISH code partition including		
SKL-U binary file SKL-H Path to your ISH firmware binary file SKL-H Path to your ISH firmware binary file		Input File			SKL-Y	Path to your ISH firmware
SKL-H SKL-H Path to your ISH firmware binary file					SKI-II	binary file Path to your ISH firmware
SKL-H Path to your ISH firmware binary file						binary file
Dath to your ISH firmwore					SKL-H	Path to your ISH firmware binary file
SKL-S binary file					SKL-S	Path to your ISH firmware binary file



Table 2-14. Intel[®] FIT - Integrated Sensor Hub (Sheet 2 of 2)

Click or	n Integrated Senso	or Hub in the left tabs	menu> ISH Data is expa	anded by default:	
▼ ISH	l Data				
	Parameter	Value		Help Text	
PDT Bina	ıry File		Path to your PDT binary f	ile	
#	Parameter			Platform	Settings
3	Integrated Sensc	or Hub - ISH Data			
	PDT Binary File			SKL-Y SKL-U SKL-H SKL-S	Path for PDT Binary file Path for PDT Binary file Path for PDT Binary file Path for PDT Binary file



Table 2-15. Intel[®] FIT - Debug (Sheet 1 of 3)

	Parameter Value Help Text			elp Text	
ebug Ove	erride Pre-Production	0x0	Allows the OEM to control FW	features to assist with pre-pro	ductio
ebug Ove	erride Production Sili	0x0	Allows the OEM to control FW	features to assist with produc	tion pl
nable Inte	el(R) ME Reset Capt	No	This setting configures Intel(R)	ME behavior when it resets du	Iring C
rmware F	ROM Bypass	No	This setting enables / disables	firmware ROM bypass. Note:	This
#		Platform	Settings		
1	Deb	ug - Intel® ME Firmv	vare Debugging Overrides		0.00000000
	features to assist	with pre-production silic	atform debugging. This control h	IS NO SKL-Y	0x0000000
	effect if used on p	production silicon.		SKL-U	0x00000000
	Bit 0: Disable DR	AM_INIT_DONE (defau	It timeout 60 seconds)	SKL-N	0x00000000
	Bit 1: Disable Hos	st Reset Timer		SILE S	0,00000000
	Bit 2: Disable CPU	U_RESET_DONE timeou	ıt		
	Bit 3: Reserved				
	Bit 4: Disable Inte	el® ME Power Gating			
	Bit 5: Reserved				
	Bit 6: Secure Boo	ot debug hook. Used to	shorten wait time before ENF sh	utdown.	
	Bit 7: Force real F	FPFs on preproduction	(default is to use flash)		
	Bit 8: Secure Boo	ot debug hook. Used to	reduce S3 or FFS optimization tr	es.	
	Bit 9: Reserved				
	Bit 10: Override	power package to alway	ys enter M3.		
	Note: Certain opt	tions do not work when	the descriptor is locked.		
	Debug Override	Production Silicon -	Allows the OEM to control FW fea	tures to SKL-Y	0x0000000
	assist with produc	ction platform debuggin	g.	SKL-U	0x0000000
	Bit O: Extend DRA	AM_INIT_DONE timeou	t to 30 minutes (default timeout	15 SKL-H	0x0000000
	seconds)			SKL-S	0x0000000
	Bit 1: Disable Hos	st Reset Timer			
	Bit 2: Disable CPL	U_RESET_DONE timeou	it		
	Note: Certain opt	tions do not work when	the descriptor is locked.		
	Enable Intel® M	IE Reset Capture on (CLR_RST#	SKL-Y	No
	Values: Yes/No	- This setting configure	es Intel® ME behavior when it re	sets SKL-U	No
	uuring CL_KST#T	. NOLE. THE LECONTROL	active action to this setting is NO	SKL-H	No
		_		SKL-S	NO
	Firmware ROM E	Bypass		SKL-Y	No
	This setting only b	 I his setting enables / has affect when the firm 	alsables firmware ROM bypass.	NOTE: SKL-U	No
	present.		invare being used has KOW Bypa	SKL-H	NO
	prosenti			SKL-S	No
		\mathbf{T}	Connection Interface Confidu	ration is expanded by	default:

I



Table 2-15. Intel[®] FIT - Debug (Sheet 2 of 3)

#		Parameter			Settings
	Debug - Direct Connection Interface Configuration				
2					
	Direct Connect Interf	aco (DCI) Enabled			Voc
	Values: Ves /No - This	setting enables / disables the DC	Linterface used for	SKL-T	Ves
	Intel® Trace Hub debug	iging.	I Internace used for	SKL-U	Ves
				SKL	Ves
Click or	Debug in the left tabs	menu> Intel® Trace Hub Tec	hnology is expanded by	default:	103
▼ In	tel(R) Trace Hub 1	Technology 3			
	Parameter	Value		Help Text	
Intel(R)	Trace Hub Emergency	No	This setting enables / dis	sables Intel(R) Tra	ace Hub in the firmv
Intel(R)	Trace Hub Soft Enabled	No	This setting configures t	he Intel(R) Trace Hub soft enable. No	
Intel(R)	Trace Hub Debug Mess	No	This setting enables / dis	sables the Intel(R) Trace Hub debug n	
Unlock T	Unlock Token This allows the OEM to		This allows the OEM to i	nput an Unlock To	ken binary file for d
#		Parameter		Platform	Settings
3	3 Intel® Trace Hub Emergency Mode Enabled Values: Yes /No - This setting enable / disables Intel® Trace Hub in the firmware			SKL-Y SKL-U	No No
	base image.			SKL-H SKL-S	No No
	Intel® Trace Hub Soft Enabled Values: Yes/No - This setting configures the Intel® Trace Hub soft enable. Note: When enabling this setting you also need to enable Intel® Trace Hub Debug			SKL-Y SKL-U SKL-H	No No No
	Messages setting for pro	oper operation.		SKL-S	No
	Intel® Trace Hub Debug Message Enabled			SKL-Y	No
	Values: Yes/No - This setting enables/disables the Intel® Trace Hub debug			SKL-U	No
	messages. Note: When enabling this setting you also need to enable Intel® Trace Hub Soft Enable setting for proper operation.			SKL-H	No
				SKL-S	No
	Unlock Token				
	This allows the OEM to input an Unlock Token binary file for closed chassis debug.				
Click or	n Debug in the left tabs	menu> Intel® IDLM is expan	ded by default:		
▼ IDLM 4					
	Parameter	Value		Heln Tex	t
IDLM Binary This allows an IDLM bi			inary to be merge	- ed into output image	



Table 2-15. Intel[®] FIT - Debug (Sheet 3 of 3)

#	Parameter	Platform	Settings
4	Debug - Intel® IDLM		
	Intel® IDLM This allows an IDLM binary to be merged into output image built by Intel® FIT.		



Table 2-16. Intel[®] FIT - CPU Straps (Sheet 1 of 3)

Click on CPU Straps in the left tabs menu> CPU Straps are expanded by default:

 CPU Straps 		
Parameter	Value	Help Text
Disable Hyperthreading	No	This setting control enabling / disabling of Hyper threading. Note: This strap is in
Number of Active Cores	All	This setting controls the number of active processor cores. Note: This strap is in
BIST Initialization	No	This setting determines if BIST will be run at platform reset after BIOS requested
Flex Ratio	0x0	This setting controls the maximum processor non-turbo ratio. Note: This strap is
Processor Boot Max Frequency	Yes	This setting determines if the processor will operate at maximum frequency at p
JTAG Power Disable	No - No JTAG Power on C10 an	This setting determines if JTAG power will be maintained on C10 or lower power
SA Power Plane Topology	0x2	This setting determines the SA power plane topology. See Processor EDS for det
SA VR Type	SVID	This setting determines the SA core domain VR type. See Processor EDS for det
IA Power Plane Topology	0x0	This setting determines the IA power plane topology. See Processor EDS for det
IA Power Plane VR	SVID	This setting determines the IA core domain VR type. See Processor EDS for deta
Ring Power Plane Topology	0x0	This setting determines the Ring power plane topology. See Processor EDS for d
Ring VR Type	SVID	This setting determines the Ring domain VR type. See Processor EDS for details.
GT_US Power Plane Topology	0x1	This setting determines the GT Unslice power plane topology. See Processor EDS
GT_US VR Type	SVID	This setting determines the GT Unslice domain VR type. See Processor EDS for d
GT_S Power Plane Topology	0x1	This setting determines the GT slice power plane topology. See Processor EDS for
GT_S VR Type	SVID	This setting determines the GT slice domain VR type. See Processor EDS for det
SVID Presence	SVID Present	This setting determine if SVID rails are present on the platform. See Processor B
Platform IMON Disable	0x0	This strap should be left at the recommended default setting.
eOPIO Power Plane Topology	0x0	This setting determines the eOPIO power plane topology. See Processor EDS for
eOPIO VR Type	Fixed VR	This setting determines the eOPIO domain VR type. See Processor EDS for detail
EDRAM Power Plane Topology	0x0	This setting determines the EDRAM power plane topology. See Processor EDS fo
EDRAM VR Type	Fixed VR	This setting determines the EDRAM domain VR type. See Processor EDS for deta
SE Key Mode	0	Note: This strap should be left at the recommended default setting.



Table 2-16. Intel[®] FIT - CPU Straps (Sheet 2 of 3)

#	Parameter	Platform	Settings
	CPU Straps - CPU Straps		
	Disable Hyperthreading	SKL-Y	No
	Values: Yes/No	SKL-U	No
	This setting controls enabling or disabling of Hyper threading. Note: This strap is	SKL-H	No
	intended for debugging purposes only. See BIOS Spec for more details on enabling / disabling Hyperthreading.	SKL-S	No
	Number of Active Cores	SKL-Y	All
	Values: All, 1, 2, 3, 4	SKL-U	All
	This setting controls the number of active processor cores. Note: This strap is	SKL-H	All
	enabling or disabling processor cores.	SKL-S	All
	BIST Initialization	SKL-Y	No
	Values: Yes/No	SKL-U	No
	This setting determines if BIST will be run at platform reset after BIOS requested	SKL-H	No
	Note: This strap is intended for debugging purposes only.	SKL-S	No
	Flex Ratio	SKL-Y	0x0
	This setting controls the maximum processor non-turbo ratio. Note: This strap is	SKL-U	0x0
	intended for debugging purposes only. See BIOS Spec for more details on	SKL-H	0x0
	maximum processor non-turbo ratio configuration.	SKL-S	0x0
	Processor Boot Max Frequency	SKL-Y	Yes
	Values: Yes/No	SKL-U	Yes
	This setting determines if the processor will operate at maximum frequency at	SKL-H	Yes
	power-on and boot. Note: This strap is intended for debugging purposes only.	SKL-S	Yes
	JTAG Power Disable	SKL-Y	No
	Values: Yes - JTAG Power on C10 and Lower/No - No Power on C10 and	SKL-U	No
	This setting determines if ITAG nower will be maintained on C10 or lower nower	SKL-H	No
	states. Note: This strap is intended for debugging purposes only.	SKL-S	NO
	SA Power Plane Topology	SKL-Y	0x2
	This setting determines the SA power plane topology. See Processor EDS for	SKL-U	0x2
	details. Note: This strap should be left at the recommended default setting.	SKL-H	0x2
		SKL-S	0x2
	SA VR Type	SKL-Y	SVID
	Value: SVID/FIXed VR	SKL-U	SVID
	details.	SKL-TI	Fixed VP
	LA Dower Diano Topology	SKL-S	
	This setting determines the LA nower plane topology. See Drocessor EDS for	SKL-1	0x0
	details. Note: This strap should be left at the recommended default setting.	SKL-U	0x0
	· · · · · · · · · · · · · · · · · · ·	SKL-S	0x0
	IA Power Plane VR	SKI-Y	SVID
	Value: SVID/Fixed VR	SKL-U	SVID
	This setting determines the IA core domain VR type. See Processor EDS for	SKL-H	SVID
	details.	SKL-S	SVID
	Ring Power Plane Topology	SKL-Y	0x0
	This setting determines the Ring power plane topology. See Processor EDS for	SKL-U	0x0
	details. Note: This strap should be left at the recommended default setting.	SKL-H	0x0
		SKL-S	0x0
	Ring VR Type	SKL-Y	SVID
	Value: SVID/Fixed VR	SKL-U	SVID
	This setting determines the Ring domain VR type. See Processor EDS for details.	SKL-H	SVID
		SKL-S	SVID



Table 2-16. Intel[®] FIT - CPU Straps (Sheet 3 of 3)

#	Parameter	Platform	Settings
	GT_US Power Plane Topology	SKL-Y	0x1
	This setting determines the GT Unslice power plane topology. See Processor EDS	SKL-U	0x3
	for details. Note: This strap should be left at the recommended default setting.	SKL-H	0x3
		SKL-S	0x3
	GT_US VR Type	SKL-Y	SVID
	Value: SVID/Fixed VR	SKL-U	SVID
	This setting determines the GT Unslice domain VR type. See Processor EDS for	SKL-H	SVID
	details.	SKL-S	SVID
	GT_S Power Plane Topology	SKL-Y	0x1
	This setting determines the GT slice power plane topology. See Processor EDS for	SKL-U	0x1
	details. Note: This strap should be left at the recommended default setting.	SKL-H	0x1
		SKL-S	0x1
	GT_SVR Type	SKL-Y	SVID
	Value: SVID/Fixed VR	SKL-U	SVID
	This setting determines the GT slice domain VR type. See Processor EDS for	SKL-H	SVID
	details.	SKL-S	SVID
	SVID Presence	SKL-Y	SVID Present
	Value: SVID Present/SVID Not Present	SKL-U	SVID Present
	This setting determines if SVID rails are present on the platform. See Processor	SKL-H	SVID Present
	EDS for details.	SKL-S	SVID Present
	Platform IMON Disable	SKL-Y	0x0
	This strap should be left at the recommended default setting.	SKL-U	0x0
		SKL-H	0x1
		SKL-S	0x1
	eOPIO Power Plane Topology	SKL-Y	0x0000000
	This setting determines the eOPIO power plane topology. See Processor EDS for	SKL-U	0x0000000
	details. Note: This strap should be left at the recommended default setting.	SKL-H	0x0000005
		SKL-S	0x00000005
	eOPIO VR Type	SKL-Y	Fixed VR
	Value: SVID/Fixed VR	SKL-U	Fixed VR
	This setting determines the eOPIO domain VR type. See Processor EDS for details.	SKL-H	Fixed VR
		SKL-S	Fixed VR
	EDRAM Power Plane Topology	SKL-Y	0x0000000
	This setting determines the EDRAM power plane topology. See Processor EDS for	SKL-U	0x0000000
	details. Note: This strap should be left at the recommended default setting.	SKL-H	0x00000004
		SKL-S	0x00000004
	EDRAM VR Type	SKL-Y	Fixed VR
	Value: SVID/Fixed VR	SKL-U	Fixed VR
	This setting determines the EDRAM domain VR type. See Processor EDS for	SKL-H	Fixed VR
	details.	SKL-S	Fixed VR
	SE Key Mode	SKL-Y	0
	Note: This strap should be left at the recommended default setting.	SKL-U	0
		SKL-H	0
		SKL-S	0



# Parameter		CRB	Values
📲 Intel ® Flash Image T	icol		
File Build Help			
	🛃 🔕 🔫 📶 H Serie	s Chipset 👻 Intel (R) Q170 - Desktop	•
Flash Layout	▼ GbE Region		
Flash Settings	Parameter	Value	Help Text
Intel (R) ME Kernel	Length	0	
Intel (R) AMT	GbE Binary File	E:/Kits/CSME_11.0_Consumer.	
Platform Protection	GbE Region Enable	Enabled	
Integrated Clock Contro	ller		
Networking & Connectiv	ity Intel(R) ME Region		
Flex I/O	Parameter	Value	Help Text
Internal PCH Buses	Length	0	•
GPIO	Intel(R) ME Binary File	E:/Kits/CSME_11.0_Consumer.	. •
Power	PDD Pegion		
Integrated Sensor Hub	• FOR Region		
Debug	Parameter	Value	Help Text
CPU Straps	I enoth	n	
Loading C:/Users/man Loading C:/Users/man Loading C:/Users/man Loading C:/Users/man Loading C:/Users/man Loading C:/Users/man Error 7: File not found. Loading default.config	hayo/Desktop/fit_ww35.2/newfilet hayo/Desktop/fit_ww35.2/newfilet hayo/Desktop/fit_ww35.2/newfilet hayo/Desktop/fit_ww35.2/newfilet hayo/Desktop/fit_ww35.2/newfilet hayo/Desktop/fit_ww35.2/spt_h_fit E:\Kits\CSME_11.0_Consumer_ instion	mpl.xml mpl.xml mpl.xml mpl.xml mpl.xml t_cfg_a0.xml 11.0.0.1075\CSME_11.0_Consumer_11.0	.0.1075\/mage Components\/ME\H\meimage.bin
Green Buil	d button	Can also select CT	RI + B or Build > Build Image from the menu b
		along the top of th	ne screen
2 Console sh build and p	nows status of path where saved		

Table 2-17. Intel[®] FIT - Build Image



3 Programming SPI Flash Devices and Checking Firmware Status

Now that the Flash image file has been created, it can be programmed into the SPI Flash device(s) of the target machine. For platforms that don't boot, a Flash Chip Programmer will be required. For platforms that can boot to DOS or Windows*, the Intel® FPT can be used.

3.1 Flash Burner/Programmer

The specific use of a Flash burner/programmer is beyond the scope of this document. Here are some general steps that may be followed:

1. Navigate to your **Output Directory** (as specified in Table 2-2) where your generated SPI Flash image(s) are saved. It is assumed that this image file is named **outimage.bin**.

If two total SPI Flash devices were specified during the build process, then additional image files will be saved, one for each SPI Flash device. These files are assumed to be named **outimage(1).bin** and **outimage(2).bin**.

 Utilize a Flash burner/programmer to program the image(s). For multiple SPI Flash devices, the images are numbered sequentially to correspond to the first and second SPI Flash device accordingly.

3.1.1 In-Circuit SPI Flash Programming for CRB

Mobile CRBs have the SPI Flash devices soldered down. As a result, to program the SPI Flash for mobile CRBs, follow these steps:

- 1. Leave CRB powered on.
- 2. Connect Flash Programmer (such as DediProg SF600) header to connector **J3F3** which is labelled **"SPI TPM"**. Make sure to line up pin 1 on the header.
- 3. Program the first image [outimage(1).bin] to the CRB.
- 4. In Dediprog software, select application memory chip 2 button and load second image if created.
- 5. Program the second image [outimage(2).bin] to the CRB if created.
- 6. Once programming is complete, disconnect the Flash Programmer header. Power off and unplug CRB. Remove cell coin battery, wait approximately 10 seconds. Replace cell coin battery, plug CRB back in and power on.

3.2 Flash Programming Tool (Intel[®] FPT)

Intel® FPT can be used to substitute for a Flash burner/programmer, provided the system is capable of booting to a DOS or Windows* OS.

Note: Intel[®] FPT will automatically disable the Intel[®] ME or EFI prior to flashing the image to the platform.



Intel[®] FPT DOS Version

The DOS versions supported by Intel® FPT are: DOS, Free DOS, and DRMK DOS. Use the following steps to program the SPI Flash devices,

- 1. Copy all the files in the "(root)\Tools\System Tools\Flash Programming Tool\DOS" directory to the root directory of a bootable USB key.
- 2. Navigate to your **Output Directory** (as specified in Table 2-2) where your generated SPI Flash image(s) are saved. It is assumed that this image file is named **outimage.bin**. Copy this image file to the root directory of the USB key.
- 3. Boot the target system to DOS and change to the root directory of the bootable USB key. At the DOS prompt type:

fpt.exe -i

The system should respond with the number of SPI Flash devices available. For example:

```
--- Flash Devices Found ---
W25Q64BV ID:0xEF4017 Size: 8192KB (65536Kb)
W25Q64BV ID:0xEF4017 Size: 8192KB (65536Kb)
```

Note: If the SPI Flash device does not currently contain a descriptor it may report only a single device.

4. Program the SPI Flash image to the Flash device(s) by issuing the following command at the prompt:

fpt.exe -f outimage.bin

If the programming was successful, then the following message will be shown.

FPT Operation Passed

If the programming was **NOT** successful, then repeat this step to try again. If programming problems persist, then check the SPI Flash devices and platform hardware.

5. Execute a platform global reset using Intel FPT -greset. Next go to Section 3.3 to check the Intel ME Firmware status.

3.2.1 Intel[®] FPT Windows* Version

The Windows* OS versions supported by Intel® FPT are: Windows* PE 64, Windows* 7, Windows* 8/8.1. There are two versions of Intel® FPT for Windows*: a 32-bit version and a 64-bit version. Most Windows* OS, Windows* 7 (32-bit or 64-bit), Windows* 8/8.1 (32-bit or 64-bit) can use Windows* version of Intel® FPT. However, Windows* OS which do not support 32 bit compatible mode (Win PE 64-bit) **must use** Intel® FPT Windows* 64-bit version due to compatibility issues.



Use the following steps to program the SPI Flash devices,

- Navigate to your Output Directory (as specified in Table 2-2) where your generated SPI Flash image(s) are saved. It is assumed that this image file is named outimage.bin. Copy this image file to Intel® FPT directory located at "(root) \Tools\System Tools\Flash Programming Tool\Windows".
- 2. Boot the target system to Windows* and open a Command Prompt window. In this window, change to the Intel® FPT directory and at the prompt type:

fptw.exe -i

The system should respond with the number of SPI Flash devices available. For example:

```
--- Flash Devices Found ---
W25Q64BV ID:0xEF4017 Size: 8192KB (65536Kb)
W25Q64BV ID:0xEF4017 Size: 8192KB (65536Kb)
```

Note: If the SPI Flash device does not currently contain a descriptor it may report only a single device.

3. Program the SPI Flash image to the Flash device(s) by issuing the following command at the prompt:

fptw.exe -f outimage.bin

If the programming was successful, then the following message will be shown.

FPT Operation Passed

If the programming was **NOT** successful, then repeat this step to try again. If programming problems persist, then check the SPI Flash devices and platform hardware.

4. Use fptw.exe -greset to perform a G3 power cycle. Next go to Section 3.3 to check the $Intel^{®}$ ME Firmware status.

3.3 Checking Intel[®] ME Firmware Status

Use the following steps to check the platform health and Intel[®] ME FW status,

- 1. Copy the file **MEInfo.exe** in the "(root)\Tools\System Tools\MEInfo\DOS" directory to the root directory of a bootable USB key.
- 2. Boot the target system and use F2 or Del to enter the BIOS setup menu. Load default values for BIOS (on Intel[®] CRBs press F3 to load default values). Save and reboot (on Intel[®] CRBs press F4 and select Yes).
- 3. Boot the target system to DOS and change to the root directory of the bootable USB key. At the DOS prompt type:

MEInfo.exe -fwsts



The system should respond with a message similar to below.

```
Intel® MEInfo Version: 11.0.0.xxxx
Copyright(C) 2005 - 2014, Intel Corporation. All rights reserved.
FW Status Register1: 0x1E000255
FW Status Register2: 0x60002306
FW Status Register3: 0x00000300
FW Status Register4: 0x00004001
FW Status Register5: 0x00000101
FW Status Register6: 0x03C00FC9
  Current State: Normal
  ManufacturingMode: Enabled
                                       Valid
  OperationalState:
  FlashPartition:
                                                M0 with UMA
 OperationalState:

InitComplete: Complete

BUPLoadState: Success

ErrorCode: No Error

ModeOfOperation: N

Phase: HOSTCOMM Module

LCC: Valid OFM dat
                                               Normal
                            Valid OEM data, ICC programmed
  ICC:
  SPI Flash Log:
                                                       Not Present
  ME File System Corrupted:
                                                                    No
  FPF and ME Config Status:
                                                                    Not committed
```

As in the above example if there are NO errors shown, then

- your platform's health is good
- Intel[®] ME FW has successfully initialized
- Intel[®] ME FW is operating normally

Note: This section is only intended to show how to use the MEInfo.exe tool for checking firmware status. For full usage and capabilities of the MEInfo.exe tool, please see the System Tools User Guide.



3.4 Common Bring Up Issues and Troubleshooting Table

Table 3-1. Common Bring Up Issues and Troubleshooting Table

Problem / Issue	Solution / Workaround		
System does not boot to DOS	 By default, the system will boot to EFI Shell. To boot to DOS, 1. Enter BIOS menu, then go to the 'Boot' screen 2. Change 'Boot Option #1' to be your USB key (ensure USB key is formatted to be DOS bootable) 3. Press 'F4' to save settings and reboot 		
Hear 3 beeps when platform powers on	 Possible device is disconnected or device not found, check platform power and MCP fan power connectors DIMM memory modules (if applicable for memory down modules USB devices (keyboard, mouse, USB key) may be plugged into inactive USB port missing/incorrect jumpers missing or poorly socketed MCP 		
No display on monitor	Ensure Corporate FW SKU supports integrated graphics. Try external graphics card.		
USB device not detected or does not work	d USB device may be plugged into inactive USB port		
System does not boot (Post Code 00)	 Incorrect Flash image – possible reasons: wrong FW selected during Flash image build process wrong Flash size selected Re-build image with correct settings and re-flash using Flash burner. 		

§§



4 Intel[®] ME Firmware Features -Details and Settings

4.1 Basic Intel AMT functionality testing

The following information outlined in this section will allow you to verify basic functionality for $Intel^{\ensuremath{\mathbb{R}}}$ AMT and WebUI features on the platform.

Table 4-1. Building and Flashing Image to Target Platform

 Building and Flashing Image to Target Platform

 Step1: Create the SPI Flash binary image using Intel® FIT using the steps outlined in Section 2.

 Step2: Flash the SPI binary image created to the target platform with Intel® FPT using the steps outlined in Section 3



Table 4-2. Basic Intel[®] AMT Testing Steps (Sheet 1 of 5)

Screen	#	Setup / Testing Steps
Press [Enter] to directly boot. Press [F2] to enter setup and select boot options. Press [F7] to show boot menu options. Press [CTRL+P] to enter the MERs Setup Menu. Press [Pause] to pause and <any key=""> to continue booting.</any>	1	Boot the system and verify that you are able to see the MEBx splash screen and the <ctrl-p< b="">> prompt is presented. Next Enter the MEBx using <ctrl-p< b="">></ctrl-p<></ctrl-p<>
Intel (R) Management Engine BIOS Extension v11.0.0.0002/Intel (R) ME v11.0.0.1075 Copyright (C) 2003-14 Intel Corporation. All Rights Reserved MAIN MENU MEEN Login > Intel (R) ME General Settings > Intel (R) AMT Configuration MEEN Exit Intel (R) ME Password Intel (R) ME Password (T11=Move Highlight (Enterl-Select Entry (Escl=Exit	2	Select MEBx Login and hit < Enter >. Type in the default MEBx password ' admin ' at the ' Intel® ME Password ' prompt as shown and hit < Enter >.


Table 4-2. Basic Intel[®] AMT Testing Steps (Sheet 2 of 5)

Screen	#	Setup / Testing Steps
Intervol Intervol Copyright (O 2003-14 Intel Corporation All Rights Reserved MIN HERU	3	Next you will be presented with the ' Intel® ME New Password ' prompt and hit < Enter >. Example Password: Admin` 12
Intel (B) Management Engine BIDS Extension v11.0.0.0002/Intel (D) ME v11.0.0.1075 Copyright (D) 2003-14 Intel Corporations. All Rights Reserved NAIN MENU FEES Logic Intel (D) ME General Settings Intel (D) ME Configuration MEBx Exit User ify password Intel (D) ME Password (14)-More Highlight Enterl-Select Entry Exc1-Exit	4	Next you will be prompted to Verify the new password again. Re-Enter your new password and hit < Enter >. Re-Enter Example Password: Admin`12



Table 4-2. Basic Intel[®] AMT Testing Steps (Sheet 3 of 5)

	#	Setup / Testing Steps		
Intel (K) Management Engine Copyright (C) 2003	BIDS Extension v11.0.0.0002/Intel(R) ME v11.0.0.1075 -14 Intel Corporation. All Rights Reserved MTEL(R) AMT CONFIGURATION			
Manageability Feature Selection > SOL/Storage Redirection/KM > User Consent Password Policy > Network Setup Activate Network Access Unconfigure Network Access > Remote Setup And Configuration > Power Control	<enabled> (Impline)</enabled>	5	Arrow down to Intel(R) AMT Configuration and press enter. Arrow down to Unconfigure Network Access and choose <full Unprovision></full 	
Intel (B) Hanagement Engine i Copyright (C) 2003. In Manageability Feature Selection > SUL/Storage Redirection/KM > User Consent Passward Policy > Network Setup fictivate Network Access Unconfigure Network Access Unconfigure Network Access Nemote Setup And Configu > Power Control > Power Control	IIIOS Extension v11.0.0.0002/Intel (B) NE v11.0.0.1075 14 Intel Corporation. All Rights Reserved IIII (R) AHI CONFIGURATION Claubled) ofingtime> CONTION ork settings including network ACLs to factory defaults. Continue: (Y/70) 6 er>-Complete Entry Escl-Discard Changes	6	Choose 'Y' to reset to defaults. Screen may flicker, once Full Unprovision is highlighted once again, go to next step.	



Table 4-2. Basic Intel[®] AMT Testing Steps (Sheet 4 of 5)

Screen	#	Setup / Testing Steps
Intel (R) Management Engine IIIOS Extension v11.0.0.0002/Intel (R) ME v11.0.0.1075 Copyright (C) 2003-14 Intel Corporation. All Rights Reserved INTEL OD ANT CONFIGURATION Manageability Feature Selection (Eashled) 3 SEL/Storage Redirection/RM 3 User Consent Password Policy (Angulare) Network Setup Macconfigure Network Access (Full Disprovision) 3 Remote Setup And Configuration 3 Power Control (Easterland (Easterland)) 4 Power Control (Easterland) 4 Power Control (Easterland)	7	Arrow up to Activate Network access and press enter.
Intel (B) Hanagement Engine BIOS Extension v11.0.0.0002/Intel (B) ME v11.0.0.1075 Copyright (C) 2003-14 Intel Corporation. All Rights Reserved INTEL (O) ANT CONTIGURATION INTEL (O) ANT CONTIGURATION Manageability Peature Selection (Cnabled) SUL/Storage Redirection/NM Deer Consent Passach Policy (Ongtime) Network Setup Petuack Setup Metaork Setup Meta	8	Choose 'Y' to activate network settings and open ME network interface. System is now configured for basic testing in Admin Digest mode. DHCP and host name settings may also be added if needed for additional network options.



Table 4-2. Basic Intel[®] AMT Testing Steps (Sheet 5 of 5)

Screen	#	Setup / Testing Steps
Intel (B) Anagement Engine EIGS Extension #11.0.0.0002/Intel (B) HE #11.0.0.1075 Copyright (C) 2003-14 Intel Corporation. All Rights Reserved NUN HEN Intel (B) HE General Settings HENE Exit	9	ESC key twice to go back to main menu. Press 'Y' to exit and save changes.
сколчание нарагори. Свосствение своту сыначение		



Windows* OS Test Console	RJ45 Network (LAN) Cable	Intel® AMT Client				
		B				
Equipment:	Equipment:	Equipment:				
Laptop or desktop with a Windows* OS installed.	RJ45 Network (LAN) Cable.	Desktop or Mobile Intel® AMT Client system.				
Purpose: This will serve as the Test Console for controlling the Intel® AMT client platform.	Purpose: This will be used to connect the Intel® AMT client and the Test Console.	Purpose: This will be the test system for verification of basic Intel® AMT functionality.				
ठ्ठ	Connect the Test Console directly to the RJ45 Network (LAN) Cable.	the Intel® AMT Client system using				
RJ45	Note: If you are using a Router based networking environment for testing you will need to connect the Test Console and Intel® AMT Client inte network environment using two RJ45 Network (LAN) Cables.					

Table 4-3. What you need for Basic Intel® AMT functionality testing



Table 4-4.	Console /	Client	Intel®	AMT	functionality	testing	(Sheet	1 o	f 10)
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Screen	#	Setup / Testing Steps
The following section will walk you through testing Intel® ME / In	ntel®	AMT basic functionality
Blank Page - Windows Internet Explorer Image: Comparison of the page Image: Comparison of the page	1	Open Internet Explorer on the Test Console and input the IP address of the target platform in the following format 'http:// <ip_address>:16992'. Example: http://192.168.1.101:16992 – Static IP from Step 12 Static IP: For Static IP address configuration make sure that the Test Console and the Client (SUT) are on the same Subnet. Examples: Test Console IP: 192.168.1.100 Client (SUT) IP: 192.168.1.101 DHCP: For DHCP environments you will need to determine the IP address that was assigned to the client platform through query of the assigned IP address list in your router. Note: Make sure that Java script is enabled in your Web browser.</ip_address>
Intel® Active Management Technology - Windows Internet Explorer Intel® Active Management Technology Intel® On Intel® On Intel® Active Management Technology on this computer. Intel® On Intel® On <	13	You should be presented with the Intel® AMT WebUI login screen. Move the mouse cursor over the ' Log On ' and click it to log in.



Table 4-4.	Console /	Client	Intel®	AMT	functionality	testing	(Sheet	2 of '	10)
							· ·		-

Screen	#	Setup / Testing Steps
Intel® Active Management Technology - Windows Internet Explorer http: http: http: http: Intel® Active Management Technology intel® Active Management Technology intel® Active Management Technology intel® Active Management Technology Vindows Security intel® Active Management Technology intel® Active Management Technology Vindows Security intel® Active Management Technology Vindows Security intel® Active Age of the active a username and password. intel® Remember my credentials intel® Remember my credentials intel® Internet Protected Mode: Off internet Protected Mode: Off internet internet 	19	 You should see the security log in screen. Enter 'admin' in the user name entry field (Step 19)
Intel® Active Management Technology - Windows Internet Explorer Intel® Active Management Technology Intel®	20	Next Enter the target platform password ' Admin ` 12 ' in the password entry field (Step 20). Note: If you have selected a password which is different from Step 3 in the previous section enter that password in the entry field.



		Screen			#	Setup / Testing Steps
Intel® Active Management	Technology Windows Integrat Suplaces			~		
interio Active Management	R1.101:16992 index htm	• 0 +• × 0 8ins	<u>م</u> میں دی۔ م	<u> </u>		
Total® Active Manage	ament Technology			-		
				-		
ntel [®] Active Mana omputer: DT-CRB	igement Technology		intel			
ystem Status	System Status					
System	Power On					
Memory	IP address 192.1 IPv6 address Disat	68.1.101 fed				
vent Log	System ID 88886	8888-8887-8888-8888-87888888888888				
ower Policies	Date 3/24/2	2010				
v6 Network Settings	Time 10:05	am			Once	e login is complete you should see
stem Name Settings er Accounts	Refresh			E.	the r	main WebUI screen as shown.
	Copyright 8 2015-2019 (Hel C	orgonation. All Rights Reserved. Intel [®] Active Management Technology firmware vers	ien:730-build 1920	_		
12		<u></u>	2	-		
This:	section will test	Internet Protected Mode Off Basic ME / AMT Remote C	مين ⊀‱ ∙ ontrol functio	nal	ity ir	n the S0 power state
This	section will test	Internet Protected Mode Off Basic ME / AMT Remote C	A • tims • ontrol functio	nal	ity ir	n the S0 power state
ne This	section will test	Internet Protected Mode Off Basic ME / AMT Remote C ernet Explorer	A • ₹۱۵۵۶ • ontrol functio	onal	ity ir	n the S0 power state
ne This : E Intel® Active Manag	section will test pement Technology - Windows Intr /1921681.10116992/indei.html	Internet Protected Mode Off Basic ME / AMT Remote C erret Explorer • + + x > Bing	م بر المعرفة من المعرفة معرفة معرفة من المعرفة م معرفة معرفة من المعرفة م	nal	ity ir	n the S0 power state
ne This Intel® Active Manag © © © @ http: @ Intel® Active	section will test rement Technology - Windows Int / 1921681.101.16992/index.htm Management Technology	Internet Protected Mode Off Basic ME / AMT Remote C ernet Explorer	<u>م</u> بر 1005 ب ontrol functio	nal	ity ir	n the S0 power state
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Intel® Active Manag	Section will test sement Technology - Windows Inte '192168.1.0116992/inde.htm Management Technology Management Technology System Status Power IP address IPv6 address System ID	Internet Protected Mode Off Basic ME / AMT Remote C erret Explorer · · · · · · · · · · · · · · · · ·	A + 1005 + ontrol functio		ity ir	n the S0 power state
This Intel® Active Manag Intel® Active Manag Intel® Active Intel® Active	section will test pement Technology - Windows Int 192168.1.01.16992 inde.htm Management Technology Management		A + 1,005 + ontrol functio		ity ir	n the S0 power state
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ne Intel® Active Manag Intel® Active Manag Intel® Active Manag Intel® Active Manag Intel® Active Management Intel® A	section will test perment Technology - Windows Int 1921681.101 16992 Index.htm Management Technology Management Technology System Status Power IP address IP v6 address System ID Date Time Bafrach Bafrach		A + 1005 + ontrol functio		ity ir	n the SO power state Next select the ' Remote Contro WebUI menu option as shown.
ne Intel® Active Manag Intel® Active Manag Intel® Active Manag Intel® Active Intel® Active Intel® Active Intel® Active Intel® Active Intel® Active Intel® Active Intel® Active Intel® Active Intel® Active Intel® Activ	section will test perment Technology - Windows Inte (192168.1.01.16992/index.htm) Management Technology Management Manage		A + 1005 + ontrol functio		ity ir	Next select the ' Remote Contro WebUI menu option as shown.
ne Intel® Active Manag Intel® Active Manag Intel® Active Manag Intel® Active Manag Intel® Active Intel® Active Intel® Active Intel® Active Intel® Intel® Active Intel® Active Intel® Active Intel® Intel	section will test perment Technology - Windows Int 1 1921681.101 16992 Index.htm Management Technology Management Technology System Status Power IP address System ID Date Time Refresh Copyright © 2005-2009 Intel Co	Cn 192.168.1.101 Disabled 0000000-0000-0000-000001000501 1/4/2005 4.33 am orporation. All Rights Reserved. Intel® Active Management Technol build 1238	A tions of ontrol function P of (interior) (interi		ity ir	Next select the ' Remote Contro WebUI menu option as shown.
ne This : Intel® Active Manag Computers DT-CRB Intel® Active I Computers DT-CRB System Status Hardware Information System Processor Procesor Processor Processor Processor Processor Pr	section will test perment Technology - Windows Int / 192168110116992 index.htm Management Technology Management Technology System Status Power IP address IPx6 address System ID Date Time s Copyright © 2005/2009 Intel Co Power IPaddress System ID Date Time System ID Date Date Date Date Date Date Date Dat		A + 1,10% +		etty ir	Next select the ' Remote Contro WebUI menu option as shown.

Table 4-4. Console / Client Intel[®] AMT functionality testing (Sheet 3 of 10)



Table 4-4. Console / Client Intel [®] AMT functionality testing (Sheet 4 of	Table 4-4.	Console /	Client Intel®	[®] AMT functionalit	v testina	(Sheet 4	of 10	n
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 Table 4-4.
 Console / Client Intel[®] AMT functionality testing (Sheet 5 of 10)



Table 4-4.	Console /	' Client In	tel [®] AMT	functionality	testing	(Sheet	6 of	10)
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		Screen		#	Setup / Testing Steps
 Intel® Active Manageme 	nt Technology - Windows Internet Explorer 188 1 101 19992 Index htm segement Technology Augement Technology System Status Prover On Providence On On One Providence On One One Providence On One One One One One One One One One		P • P • P • P • P • P • P • P • P • P •	Whe '0' tł mair The shou	n the countdown timer has reached he WebUI should return to the initial n menu screen as shown. Power state under ' System Status ' Ild be showing ' On '.
This	s section will test B	asic ME / AMT Remote	Control functiona	tily i	n the Sx power state
Intel® Active Mar Intel® Active Intel® Active Intel® Active Computer: DT-CRE System Status Hardware Informat System Processor Memory Disk Event Log Remote Control Power Policies Network Sette Lus IPv6 Network Sette Lus Herwork Sette Lus Herwor	agement Technology - Windows Internet tip://192168.1101.16992/index.htm ive Management Technology e Management Technology e Management Technology g System Status Power P address System ID Date Time Refresh Copyright 8 2005-2009 Intel Corpo 6992/power.htm	Explorer	01 Image: Image: Image	24	Next select the ' Power Policies ' WebUI menu option as shown.



	Screen		#	Setup / Testing Steps
	2	5	25	Verify the target platform is configured for Sx state operations Power Policy 2 ' On in SO, ME Wake in S3, S4-5 ' as shown.
 Intel® Active Manageme Intel® Active Manageme Intel® Active Man System Status Hardware Information System Status Hardware Information System Processor Memory Disk Power Poincy Power Poincy Intervork Settings Ipv6 Hetwork Settings User Accounts 	t Technology - Windows Internet Explorer 168.1.101 16992 index.htm gement Technology aggement Technology System Status Power On IP address 192.168.1.101 IP Address Disabled System ID 0000000-0000-0000-000-000-000-000-000-	Bing P Bing P Image: State of the state of th	26	Next select the ' Remote Control ' WebUI menu option as shown.

Table 4-4. Console / Client Intel[®] AMT functionality testing (Sheet 7 of 10)



Table 4-4. Console / Client Intel[®] AMT functionality testing (Sheet 8 of 10)

Entel® Active Managem Composition of the second s	ent Technology - Windows Internet Explorer 12.168.1.101.16992/remote.htm	• • • • • • • • • • • • • • • • • • •		
Computer: DT-CRB System Status Hardware Information System Processor Memory Disk Event Log Remote Control Power Pow Jes Remote Control Power Pow Jes Network Settings System Name Settings User Accounts	Remote Control Power state: On Send a command to this computer:		You Con	should now see the ' Remote trol ' screen as shown.
one	Internet Protected Mode: Off 4	- - ★ 100% +		
Intel® Active Managem Intel® Active Managem	Internet Protected Mode: Off Internet Protected Mode: Off Internet Explorer Intechnology Internet Explorer Internet Technology Internet Technology Remote Control			
Intel [®] Active Managem Intel [®] Active Manag	Internet Protected Mode: Off Int Technology - Windows Internet Explorer 2168.1101 16992 remote htm agement Technology nagement Technology Remote Control Power state: On Send a command to this computer: Order power off Cryde power off and on* Select a boot option: Normal boot Boot from local CO/DVD drive Boot from local CO/DVD drive Boot from local Co/DVD drive Boot from local coss. Send Command		27	 Select the 'Turn power of from the listed Remote Contro options as shown. Next click on the 'Send Command' button.





Table 4-4. Console / Client Intel[®] AMT functionality testing (Sheet 9 of 10)



	Scre	en	#	Setup / Testing Steps
Intel® Active Manageme Intel® Active Manageme Intel® Active Manageme File Edit View Favorites Intel® Active Manageme Intel® Active Manageme Computer: skippy	ent Technology - Windows In oy.ent.vprodemo.com:16993/ind Tools Help lanagement Technology nagement Technology			
System Status Hardware Information System Processor Memory Disk Event Log Remote Control	System Status Power IP address IPv6 address System ID	Off 192.168.1.100 Disabled fb201300-7971-1300-20fb-7179001320fb	Whe ' 0 ' th main The I shou	n the countdown timer has reached ne WebUI should return to the initial n menu screen as shown. Power state under ' System Status ' Id be showing ' Off '.
Power Policies Network Settings IPv6 Network Settings System Name Settings User Accounts	Date Time Refresh	7/29/2014 9:30 pm		

Table 4-4. Console / Client Intel[®] AMT functionality testing (Sheet 10 of 10)

4.2 Features Supported

These options control the availability/visibility of firmware features.

In instances where a specific feature is configurable in MEBx, disabling it through the 'Features Supported' section will hide/disable that specific feature in MEBx.

The ability to change certain options is SKU dependent and some default values will be grayed out and will not be changeable depending on the SKU selected.

Note:

The Intel[®] Manageability Application setting combines several manageability technologies that are related to each other. This setting controls the following manageability technologies:

Intel[®] Active Management Technology Intel[®] Standard Management Intel[®] KVM Remote Assistance Application

Setting "Intel[®] Manageability Application Permanently Disabled?" to "Yes" will permanently disable all the features listed above without any way to enable them at a later time. The only way to re-enable these features is to completely re-burn the Intel[®] ME region with this setting value set to "No." A firmware update using **FWUpdLcI.exe** cannot re-enable these features.



A Appendix — Flash Configurations

This chapter covers only the basic information needed for clock control parameter programming. For a more detailed treatment of Mainstream - Mobile Family clocks, see Intel[®] *Skylake PCH-LP Clocks* and *Intel[®] Management Engine — Platform Compliancy Guide for ME Hardware.*

Figure A-1. Configuration "A" – Desktop/Server/Workstation or Mobile







Figure A-2. Configuration "B" — Mobile Only



Figure A-3. Configuration "C" – Desktop/Server/Workstation Only





Figure A-4. Configuration "D" — Mobile Only



§§



B Appendix — Intel[®] ICCS SKU Support Matrix

The following tables describes ICC features supported for specific PCH SKU, clock range (maximum and minimum), spread mode supported by Skylake Platform SKUs (SPT-H and SPT-LP PCH).

Note: Please refer to Skylake-LP/H Platform Controller Hub (PCH) External Design Specification (EDS) for details about Skylake Platform I/O - Chipset Clock Architecture.

For table B.1 - Min = Clock Div Max (minimum allowed frequency) and Max = Clock Div Min (maximum allowed frequency)

B.1 Intel[®] ICCS SKU Matrix - SPT-LP

Note: ICC SKU is divided into 2 categories: Basic and Enhanced. Mark "x" indicates category supported by PCH SKU.

PCH SKU	Basic	Enhanced
Premium Y		х
Premium U		x
Base U		x
Features Supported	Standard Clock Configuration	Standard Clock Configuration Adaptive Clock Configuration
Pre-Defined ICC profile supported	Standard	Standard Adaptive
Clock Range Supported	[Min-Max]=100 MHz.	BCLK [Min-Max] = 98 - 100 MHz.
SSC Supported	Down SSC: 0 - 0.5%	Down SSC: 0 - 0.5%

Table B-1. Intel[®] ICCS SKU Matrix - SPT-LP



B.2 Intel[®] ICCS SKU Matrix - SPT-H

Note: ICC SKU is divided into 3 categories: Basic ,Enhanced and Extreme. Mark "x" indicates category supported by PCH SKU.

Table B-2.	Intel®	ICCS	SKU	Matrix -	- SPT-H

PCH SKU	Basic	Enhanced	Extreme
Q170		x	
Q150		x	
B150		x	
H170		x	
Z170			x
H110		x	
QM170			x
HM170			x
CM236			x
Features Supported	Standard clock configuration	Standard clock configuration Adaptive clock configuration	Standard clock configuration Adaptive clock configuration BCLK Overclocking clock configuration
Pre-Defined ICC profile supported	Standard	Standard Adaptive	Standard Adaptive OverClocking OverclockingPlus
Clock Range Supported	[Min-Max]=100 MHz.	BCLK [Min-Max] = 98 - 100 MHz.	BCLK Over clocking [Min-Max] = 99.5 -170 MHz * BCLK Over clocking Plus [Min-Max] = 99.5 -341 MHz*
SSC Supported	Down SSC: 0 - 0.5%	Down SSC: 0 - 0.5%	BCLK Over clocking Down SSC : 0 - 0.5% BCLK Over clocking Plus Down SSC : 0 - 0.2%

*BCLK Overclocking ranges mentioned here are ranges supported by The Intel® ME FW, please make sure to choose range based on platform/HW configuration.



C Appendix — Boot Guard Configuration

C.1 Boot Guard Profiles

The following table describes the profiles available for Boot Guard Configuration.

Index	Profile Name	F	v	м	ENF	PBE	Description
o	Boot Guard Profile - No_FVME	0	0	0	00	0	This configuration will invoke Boot Guard during boot with neither Verification nor Measurement. For platforms with all the required Boot Guard components but do not wish to enable Boot Guard boot block verification protection.
1	Boot Guard VE	0	1	0	01	1	When Verification is desired but if verification fails the platform will continue to boot with the unverified IBB for a short period, to allow remediation.
2	Boot Guard VME	0	1	1	01	1	When Verification and Measured are desired and the asset protection is provided by both TPM protection and a timed remediation period.
3	Boot Guard VM	0	1	1	00	1	When Verification and Measured are desired and the asset protection is provided by TPM protection.
4	Boot Guard FVE	1	1	0	11	1	Strict Verification enforcement.
5	Boot Guard FVME	1	1	1	11	1	Strict Verification and Measured enforcement. Prevents unverified IBB from running.

Table C-1. Profile Description

C.2 Enforcement Policies

Table C-2. Enforcement Policy Description

Error Enforcement Policy (ENF)	Enforcement Mode Name	Description
0	Unrestricted Mode	Infinite time before shutdown – don't shutdown the platform, let everything run normally.
1	Remediation Mode	30 minutes before shutdown – enough time to remediate the system, e.g. update BIOS or other data on flash via host tools.
2	Reserved	
3	Restricted Mode	0 minutes before shutdown – instant shutdown policy.



C.3 OEM Profile Parameters

Table C-3. Profile Parameters Description

Parameter	Description	Settings	
Force Boot Guard ACM Enabled (F)	Force Boot Guard Boot determines if the platform starts the Force Boot Guard Boot timer. If it successfully starts it indicates success. When the Force Boot Guard timer stops, it starts the Protect Bios Environment timer, if indicated by the boot policy restrictions. Anchor ACM then jumps to the Initial Boot Block(IBB) with the Force Boot Guard Boot time stopped and the Protect BIOS enable timer running.	false - Allow the CPU to jump to the legacy reset vector if the Boot Guard Module cannot be successfully loaded. (default)true - Force the Boot Guard ACM to execute.	
Verified Boot Enabled (V)	Boot Guard cryptographically verifies the platform Initial Boot Block (IBB) using the boot policy key. On successful verification, Boot Guard executes Initial Boot Block (IBB) using the boot policy key. If the verification fails, Anchor signals or enters Remediation.	false - Platform does not perform verified boot (default) true - Platform performs verified boot	
Measured Boot Enabled (M)	Boot Guard measures the Initial Boot Block (IBB) into the TPM. Boot Guard perform no verification that the IBB is correct or from the platform manufacturer. The Slylake implementation of Boot Guard will support measurements into TPM or Intel's Platform Trust Technology.	false - Platform does not perform measured boot (default) true - Platform performs measured boot	
Protect Bios Environment Enabled (PBE)	Platform manufacturer may want Initial boot block to be protected between verification/ measurement and execution from attacks on buses and non-CPU components. Boot Guard accomplishes this by allowing the initial boot block to be verified and executed in LLC in NEM if PBE is enabled.	false - Take no actions to control the environment during execution of the BIOS components (default)true - Takes actions to control the environment during the execution of the BIOS components.	
Error Enforcement Policy (ENF)	 Boot Guard invokes the Enforcement Policy when a fatal error is encountered. The action taken by ENF is determined by the OEM set persistent policies. Like, Allowing platform to continue to boot Immediate Shutdown Shutdown with Timeout intervals When the ENF logic is invoked, PTT or TPM also disconnects. 	See Section C-2 for details.	



D Appendix — Intel[®] Platform Trust Technology

D.1 Intel[®] Platform Trust Technology

The following table describes the platform configurations supported by Intel[®] Platform Trust Technology.

Note: Intel[®] Platform Trust Technology does not support the full TPM functionality requirements and should not be used for Intel[®] vPro^m based platforms.

Table D-1. Intel[®] Platform Trust Technology Configuration table

Configuration	Platform Protection> Intel [®] PTT Configuration Intel [®] PTT initial power up state	Platform Protection> Intel [®] PTT Configuration Intel [®] PTT Supported	Platform Protection> Intel [®] PTT Configuration Intel [®] PTT Supported [FPF]	Description
Intel [®] PTT Permanently Disabled in HW via FPF	Disabled	No	No	After the End of Manufacturing command, this setting will permanently set into the FPFs contained in the MCP. If disabled, the specific MCP can never be enabled for Intel [®] PTT.
Intel [®] PTT Permanently Disabled in base firmware image	Disabled	No	Yes	This setting allows Intel [®] PTT to be set to disabled without disabling the MCP FPFs. This is the recommended option to permanently disable Intel [®] PTT on a platform.
Intel [®] PTT Ship State Disabled in base firmware image	Disabled	Yes	Yes	Intel $^{\textcircled{B}}$ PTT initially shipped in disabled mode, can be enabled by BIOS command.
Intel [®] PTT Enabled	Enabled	Yes	Yes	This is the recommended option to enable $\operatorname{Intel}^{\textcircled{B}}$ PTT on a platform.



E Appendix — Settings for RVP CRBs (B)

The following table describes the configuration settings required for RVP CRBs in the Intel[®] FIT tool. Please see SPI Programming Guide for additional details.

Table E-1. Skylake-LP RVP Board Settings - B Step

CRB Board	Setting Name	Intel [®] FIT Visible	Offset	Value
	SATA / PCIe GP Select for Port 0	No	0x168 [1:0]	0x3
	SATA / PCIe GP Select for Port 2	No	0x168 [5:4]	0x3
	USB3 / PCIe Combo Port 0 Strap	No	0x16E [1:0]	0x0
	USB3 / PCIe Combo Port 1 Strap	No	0x16E [3:2]	0x0
	GbE PCIe Port Select	Yes	0x17C [5:3]	PORT4
	SATA / PCIe Combo Port 0 Strap	Yes	0x17D [1:0]	GPIO
	SATA / PCIe Combo Port 3 Strap	Yes	0x180 [1:0]	GPIO
	USB3 / PCIe Combo Port 0	Yes	0x182 [1:0]	USB3
RVP5	USB3 / PCIe Combo Port 1	Yes	0x182 [3:2]	USB3
	SATA / PCIe Select for Port 0	No	0x18C [1:0]	0x3
	SATA / PCIe Select for Port 1	No	0x18C [3:2]	0x3
	PCIe Controller 1 (Port 1-4)	Yes	0x19D [4:3]	4x1
	PCIe Controller 2 (Port 5-8)	Yes	0x1A5 [4:3]	1x2, 2x1
	PCIe Controller 3 (Port 9-12)	Yes	0x1AD [4:3]	1x4
	PCIe Controller 3 Lane Reversal Enabled	Yes	0x1AD [2]	Yes
	XHCI Port 4 Ownership	Yes	0x1B8 [4]	XHCI
	XHCI Port 5 Ownership	Yes	0x1B8 [5]	XHCI
RVP7	SATA / PCIe GP Select for Port 0	No	0x168 [1:0]	0x0
	SATA / PCIe GP Select for Port 2	No	0x168 [5:4]	0x3
	USB3 / PCIe Combo Port 0 Strap	No	0x16E [1:0]	0x0
	USB3 / PCIe Combo Port 1 Strap	No	0x16E [3:2]	0x0
	GbE PCIe Port Select	Yes	0x17C [5:3]	PORT4
	SATA / PCIe Combo Port 1 Strap	Yes	0x17D [3:2]	SATA
	SATA / PCIe Combo Port 3 Strap	Yes	0x180 [1:0]	GPIO
	USB3 / PCIe Combo Port 0	Yes	0x182 [1:0]	USB3
	USB3 / PCIe Combo Port 1	Yes	0x182 [3:2]	USB3
	SATA / PCIe Select for Port 1	No	0x18C [1:0]	0x0
	SATA / PCIe Select for Port 2	No	0x18C [5:4]	0x3
	PCIe Controller 1 (Port 1-4)	Yes	0x19D [4:3]	4x1
	PCIe Controller 3 (Port 9-12)	Yes	0x1AD [4:3]	1x4
	PCIe Controller 3 Lane Reversal Enabled	Yes	0x1AD [2]	Yes
	XHCI Port 4 Ownership	Yes	0x1B8 [4]	XHCI
	XHCI Port 5 Ownership	Yes	0x1B8 [5]	XHCI



Note: The Intel[®] FIT default settings for Skylake-LP are based on the RVP3 CRB.

Table E-2. Skylake-H RVP Board Settings - B Step

CRB Board	Intel [®] FIT Setting Name	Intel [®] FIT Visible	Offset	Value
	SATA / PCIe GP Select for Port 0	No	0x1AC[1:0]	0x3
	SATA / PCIe GP Select for Port 1	No	0x1AC [3:2]	0x3
	SATA / PCIe GP Select for Port 2	No	0x1AC [5:4]	0x0
	SATA / PCIe GP Select for Port 3	No	0x1AC [7:6]	0x0
	SATA / PCIe GP Select for Port 4	No	0x1AD[1:0]	0x3
	SATA /PCIe Combo Port 2	Yes	0x1C1 [5:4]	GPIO
	SATA /PCIe Combo Port 3	Yes	0x1C4 [1:0]	GPIO
	SATA /PCIe Combo Port 4	Yes	0x1C4 [3:2]	SATA
	SATA /PCIe Combo Port 5	Yes	0x1C4 [5:4]	SATA
	SATA /PCIe Combo Port 6	Yes	0x1C4 [7:6]	GPIO
	Polarity Select SATA / PCI e Combo Port 2	Yes	0x1C8 [2]	SATA
	Polarity Select SATA / PCI e Combo Port 3	Yes	0x1C8 [3]	SATA
RVP8	Polarity Select SATA / PCIe Combo Port 4	Yes	0x1C8 [4]	PCIe
	Polarity Select SATA / PCIe Combo Port 5	Yes	0x1C8 [5]	PCIe
	Polarity Select SATA / PCIe Combo Port 6	Yes	0x1C8 [6]	SATA
	SATA / PCIe Select for Port 0	No	0x1D0 [1:0]	0x3
	SATA / PCIe Select for Port 1	No	0x1D0 [3:2]	0x3
	SATA / PCIe Select for Port 2	No	0x1D0 [5:4]	0x0
	SATA / PCIe Select for Port 3	No	0x1D0 [7:6]	0x0
	SATA / PCIe GPIO Polarity Port 0	No	0x1D2 [0]	0x1
	SATA / PCIe GPIO Polarity Port 1	No	0x1D2 [1]	0x1
	SATA / PCIe GPIO Polarity Port 2	No	0x1D2 [2]	0x0
	SATA / PCIe GPIO Polarity Port 3	No	0x1D2 [3]	0x0
	SATA / PCIe GPIO Polarity Port 4	No	0x1D2 [4]	0x1
	PCIe Controller 4 (Port 13-16)	Yes	0x1F9 [4:3]	1x2, 2x1
RVP9	DMI Lane Reversal	Yes	0x25E [5]	Yes
RVP11	SATA / PCIe GP Select for Port 0	No	0x1AC[1:0]	0x0
	SATA / PCIe GP Select for Port 1	No	0x1AC [3:2]	0x0
	SATA / PCIe GP Select for Port 2	No	0x1AC [5:4]	0x3
	SATA / PCIe GP Select for Port 3	No	0x1AC [7:6]	0x3
	USB3 / PCIe Combo Port 3 Strap	No	0x1B2 [7:6]	0x1
	SATA /PCIe Combo Port 2	Yes	0x1C1 [5:4]	GPIO
	SATA /PCIe Combo Port 3	Yes	0x1C4 [1:0]	GPIO
	SATA /PCIe Combo Port 4	Yes	0x1C4 [3:2]	SATA
	SATA /PCIe Combo Port 5	Yes	0x1C4 [5:4]	SATA
	USB3 / PCIe Combo Port 3	Yes	0x1C6 [7:6]	USB3



CRB Board	Intel [®] FIT Setting Name	Intel [®] FIT Visible	Offset	Value
	Polarity Select SATA / PCIe Combo Port 2	Yes	0x1C8 [2]	SATA
	Polarity Select SATA / PCIe Combo Port 3	Yes	0x1C8 [3]	SATA
	Polarity Select SATA / PCIe Combo Port 4	Yes	0x1C8 [4]	PCIe
	Polarity Select SATA / PCIe Combo Port 5	Yes	0x1C8 [5]	PCIe
	SATA / PCIe Select for Port 0	No	0x1D0 [1:0]	0x3
	SATA / PCIe Select for Port 1	No	0x1D0 [3:2]	0x3
	SATA / PCIe Select for Port 2	No	0x1D0 [5:4]	0x0
	SATA / PCIe Select for Port 3	No	0x1D0 [7:6]	0x0
	SATA / PCIe GPIO Polarity Port 0	No	0x1D2 [0]	0x1
	SATA / PCIe GPIO Polarity Port 1	No	0x1D2 [1]	0x1
	SATA / PCIe GPIO Polarity Port 2	No	0x1D2 [2]	0x0
	SATA / PCIe GPIO Polarity Port 3	No	0x1D2 [3]	0x0
	XHCI Port 10 Ownership	Yes	0x20D [1]	XHCI

Note:

The Intel[®] FIT default strap settings for Skylake-H are based on the RVP10 CRB.



F Appendix — Integrated Sensor Hub (ISH) Public Key Settings

The following table describes the configuration matrix required for ISH configuration for the Intel[®] FIT tool. Please see System Tools User Guide within ME kit, Manufacturing Test with Intel[®] Management Engine (Intel[®] ME) Firmware 11 and Intel[®] Integrated Sensor Solution on Skylake Mobile, Skylake Desktop, and Greenlow Workstation Platforms (CDI *#* 554868) for additional details.

CLSMNF = Close Manufacturing switch used with Intel[®] Flash Programming Tool (FPT)

PV = Production Version

For additional information on FPT see System Tools User Guide included with ME kit under system tools folder.

Table F-1. ISH Public Key Settings

Firmware	МСР	FPF Automatic Commit	FPF MEI command after CLSMNF (Yes/No)	FPF MEI command before CLSMNF (Yes/No)
Pre-production	Production	No	No - Not a valid combination	No - Not a valid combination
Production (PV not set)	Pre-production	No	Yes	No
Production (PV not set)	Production	No	Yes	No
Pre-production	Pre-production	No	Yes	No
Production (PV not set)	Production	Yes	No	No

Note: The Intel[®] FIT allows integration of binary files within Integrated Sensor Hub section under ISH Image and ISH Data. The Intel[®] FIT does not generate or create the required files. The table above lists configuration combinations that can be used. Please see VIP # 105658 - Intel[®] Integrated Sensor Solution 3.0 for SKL Program Alpha Corporate Milestone Release Version 3.0.0.1037 update for firmware information.