


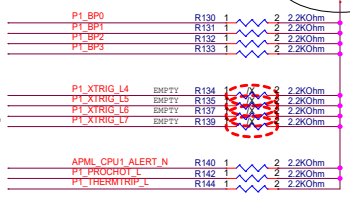
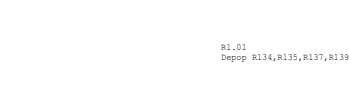
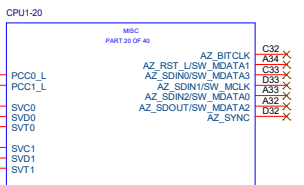
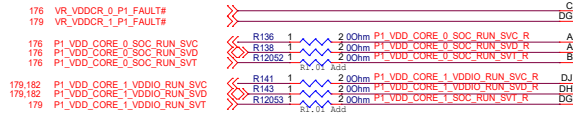
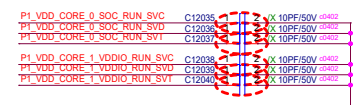
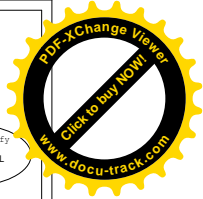
PROJECT NAME: GENOA2D32TM3 -2L+

PROJECT CODE:

Customer :

<Variant Name>

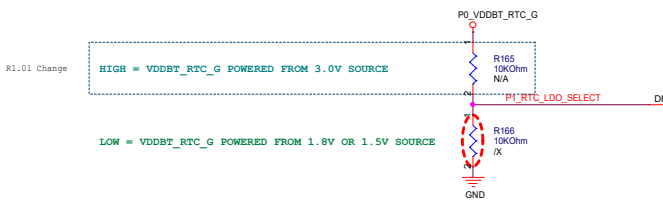
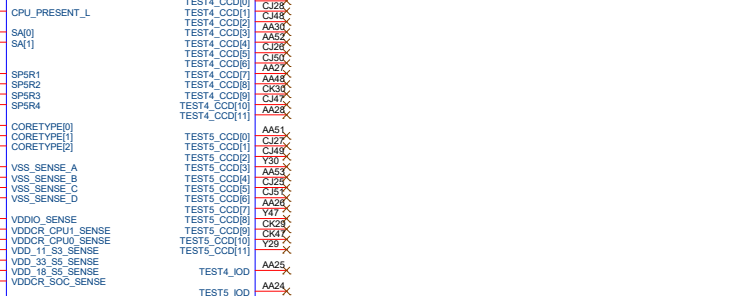
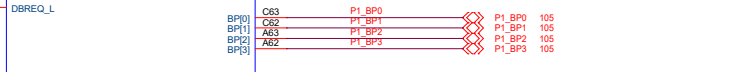
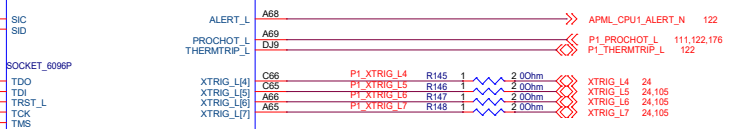
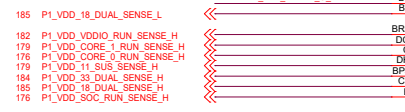
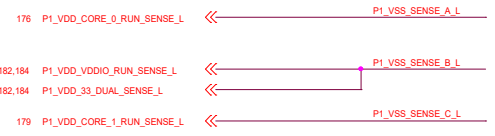
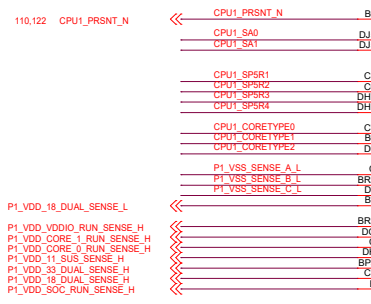
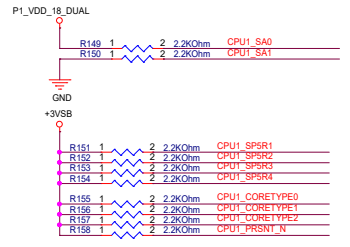
		Title : COVER
<i>ASRock Rack</i>		Engineer: Ryan Lu
Size C	Project Name GENOA2D24TM3-2L+	Rev R1.0
Date: Monday, November 21, 2022		Sheet 1 of 213



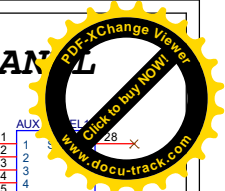
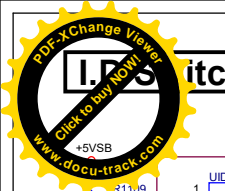
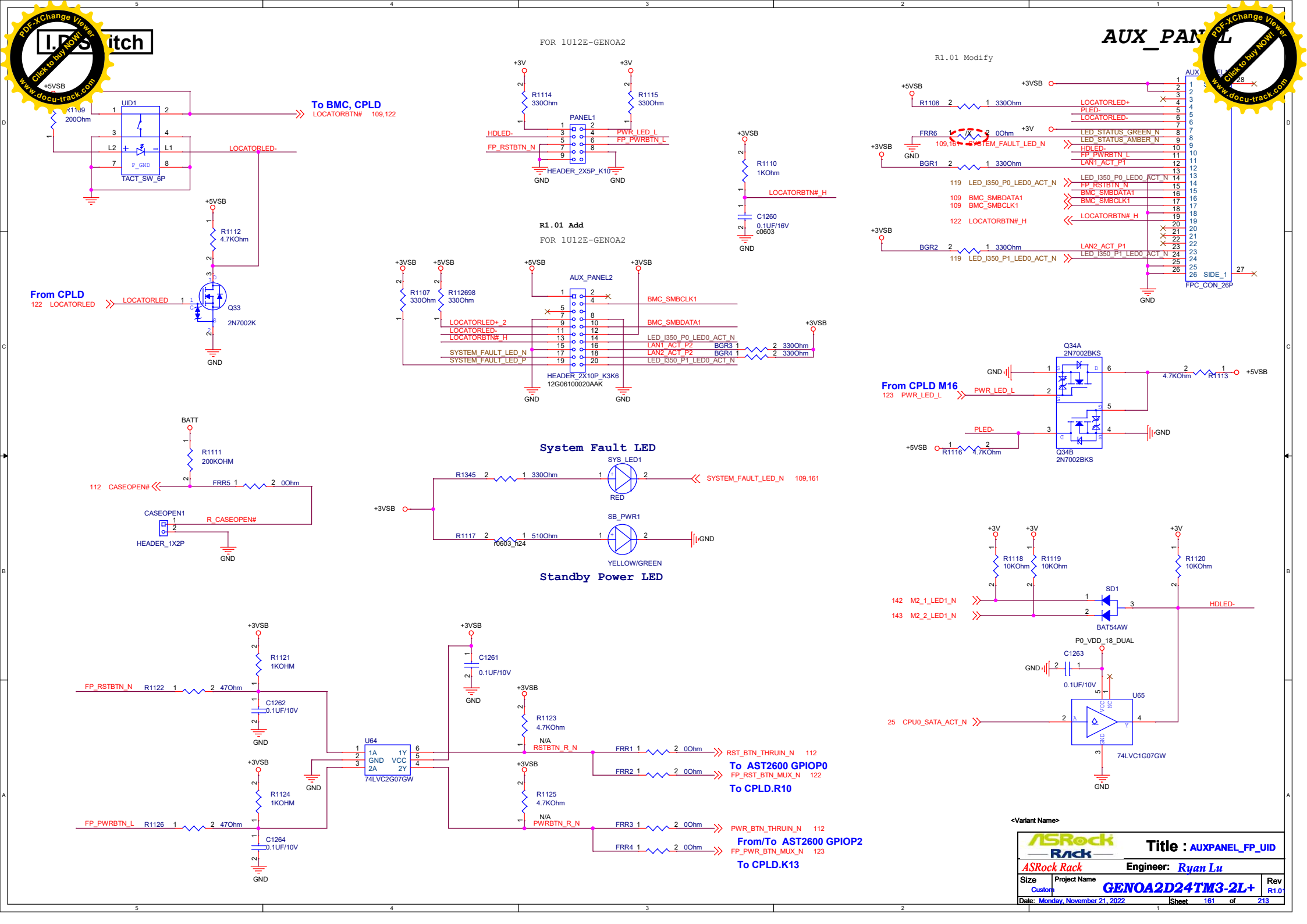
R1.01 modify
P1_VDD_18_DUAL

Socket Identifier, Strapped as follows:

SOCKET	SA[1]	SA[0]
BSP	0	0
AP	0	1

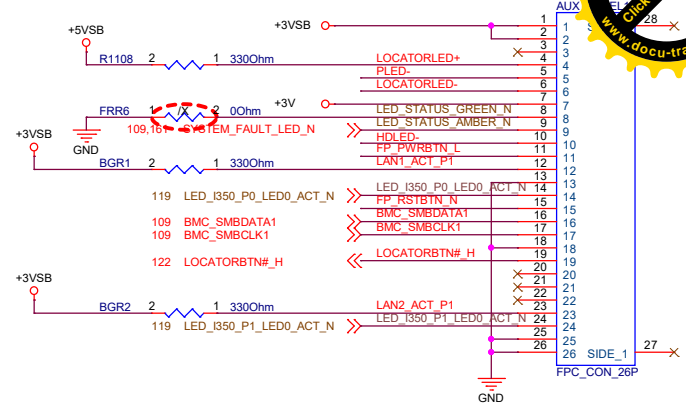


ASRock Rack
Title : CPU1 MISC 1/2
 ASRock Rack Engineer: **Ryan Lu**
 Size C Project Name **GENOA2D24TM3-2L+** Rev **R1.0**
 Date: Monday, November 21, 2022 Sheet 46 of 213

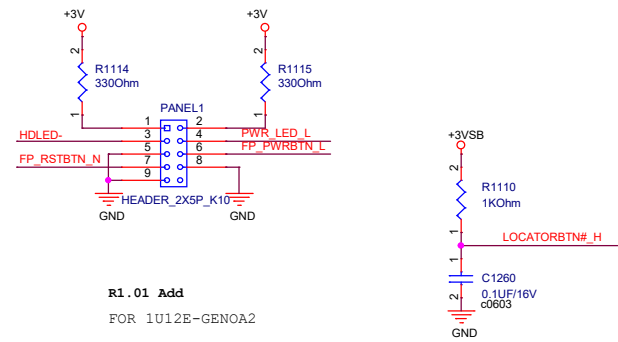


AUX_PANEL

R1.01 Modify

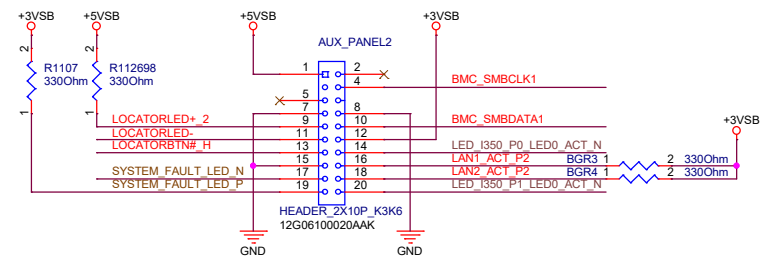


FOR 1U12E-GENOA2

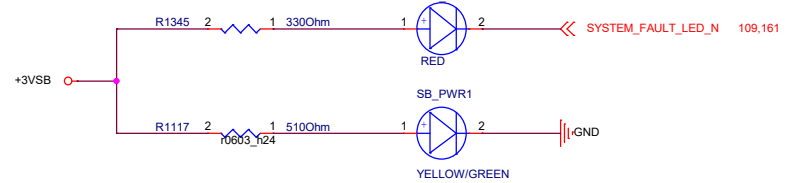


R1.01 Add

FOR 1U12E-GENOA2



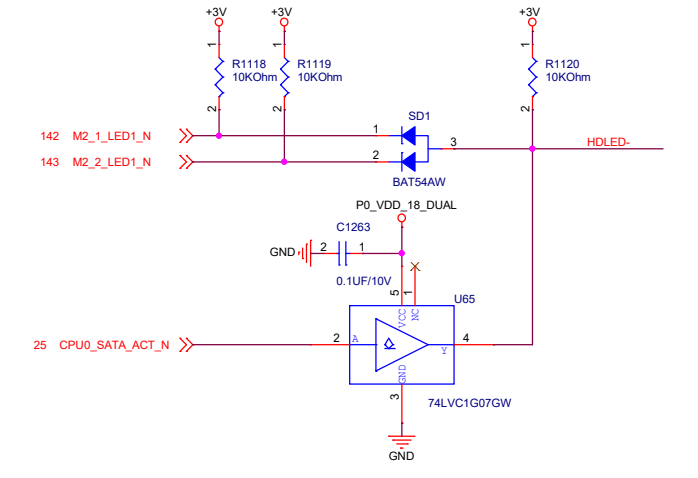
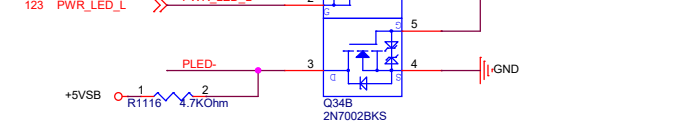
System Fault LED



Standby Power LED



From CPLD M16



To BMC, CPLD
LOCATORBTN# 109,122

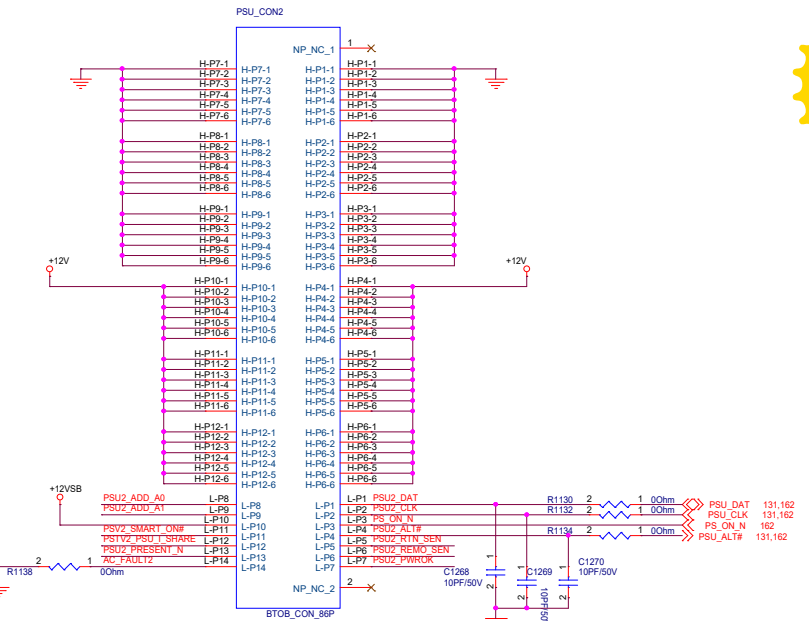
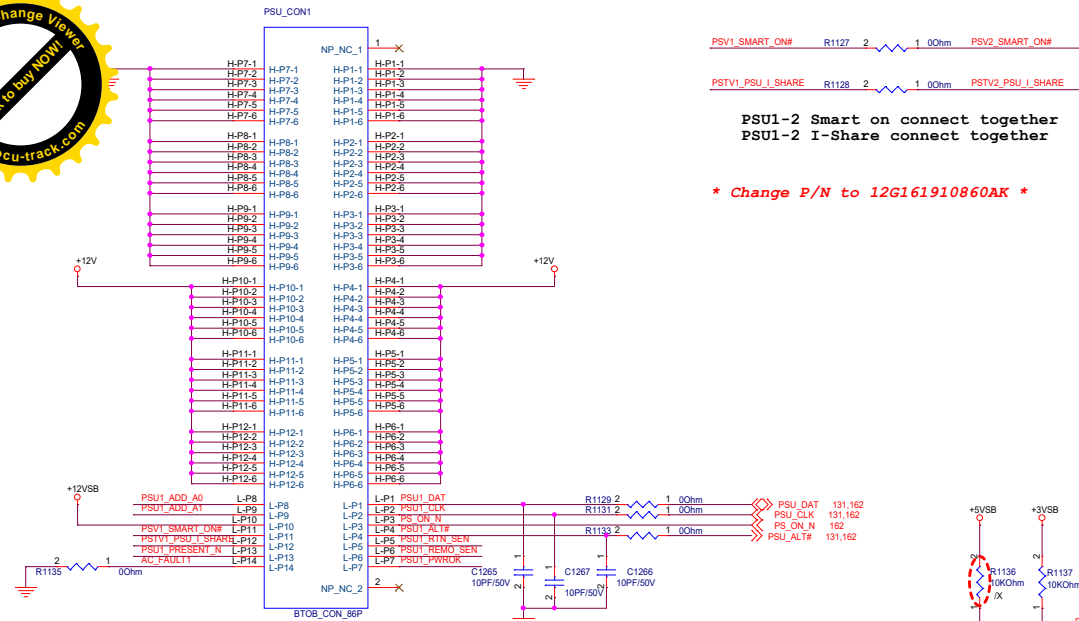
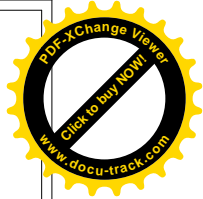
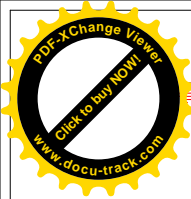
From CPLD
122 LOCATORLED

To AST2600 GPIOP
FP_RST_BTN_MUX_N 122
To CPLD.R10

From/To AST2600 GPIOP2
FP_PWR_BTN_MUX_N 123
To CPLD.K13

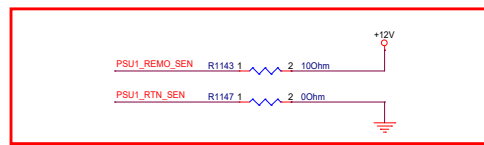
<Variant Name>

ASRock Rack		Title : AUXPANEL_FP_UID	
ASRock Rack		Engineer: Ryan Lu	
Size	Project Name	GENOA2D24TM3-2L+	
Custom		Rev R1.0	
Date: Monday, November 21, 2022		Sheet 161 of 213	

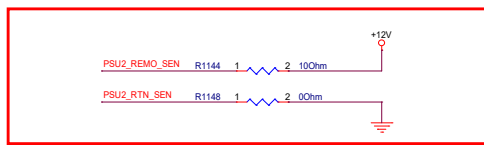


PSU1 Slave Address: 1011000X (B0/B1)

PSU2 Slave Address: 1011001X (B2/B3)



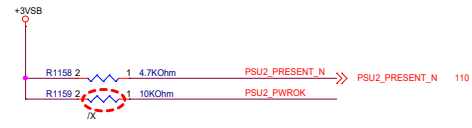
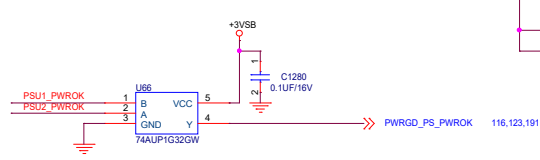
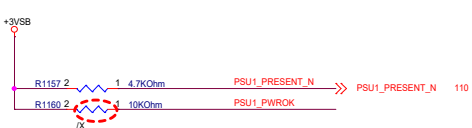
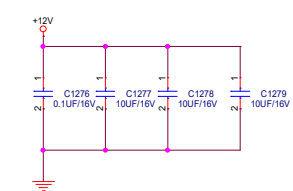
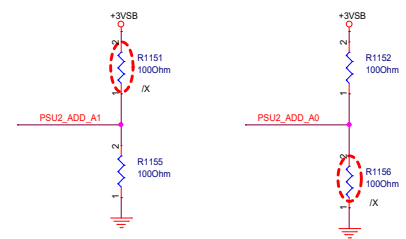
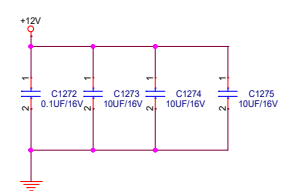
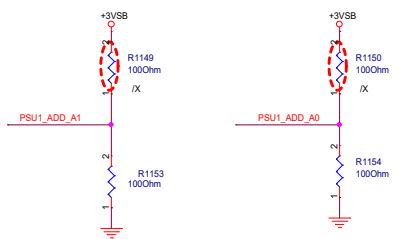
[Note] CRPS PSU spec suggest

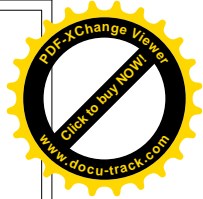
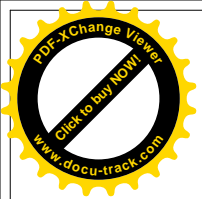


[Note] CRPS PSU spec suggest

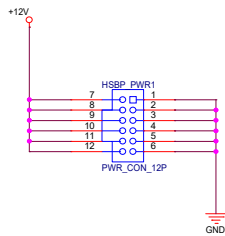
[CAD] Sense point close to PWR CONN
[Note] internal and external Remote sense resistor's ratio is 7:3, RTN_SEN connect to connector GND

[CAD] Sense point close to PWR CONN
[Note] internal and external Remote sense resistor's ratio is 7:3, RTN_SEN connect to connector GND



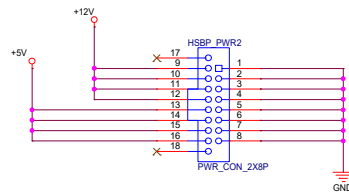


HSBP 4.2mm Power Connector

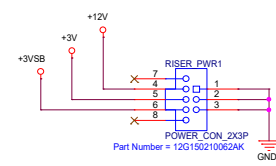


HSBP 3.0mm 12V + 5V Power Connector

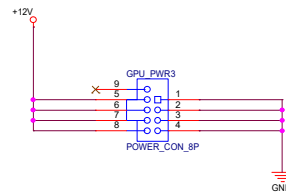
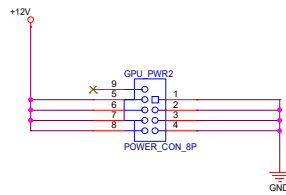
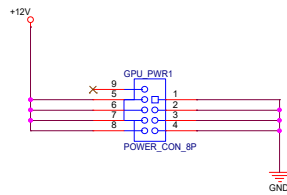
For 1U12E_BP Power Supply



PCIe CEM / U.2 SSD 3.0mm Power Connector

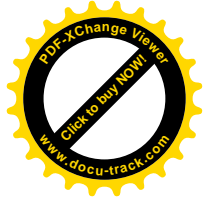
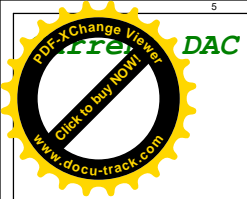


GPGPU 4.2mm Power Connector



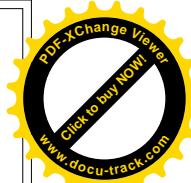
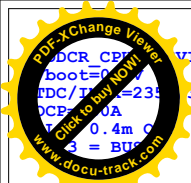
<Variant Name>

ASRock Rack		Title : HSBP PWR CONN	
ASRock Rack		Engineer: <i>Ryan Lu</i>	
Size C	Project Name GENOA2D24TM3-2L+	Rev R1.0	
Date: Monday, November 21, 2022	Sheet: 163	of	213



<Variant Name>

		Title : <Title>	
<i>ASRock Rack</i>		Engineer: <i>Ryan Lu</i>	
Size	Project Name	Rev	
Custom	GENOA2D24TM3-2L+	R1.01	
Date: Monday, November 21, 2022		Sheet	164 of 213

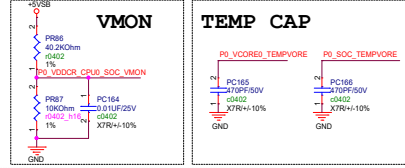


VDDCR_CPU0 (SVI3)
 Vboot=0.9V
 TDC/IMax=105A/130A
 OCP=170A
 SVI3 = BUS#1

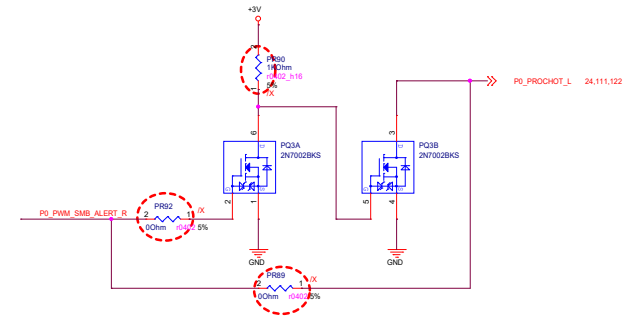
RAA229260 (SVI3)
 ISL PWM controller
 VDDCR_CPU0 + SOC = 6phase + 3phase
 PMBUS_ADDR = 61
 Config ID = 1

RAA229260 Part number change to 06G113204030AK
 Old part number had an address issue

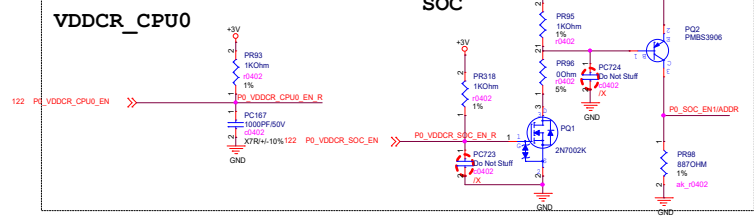
PO_VCORE0_PWM1	1	PWM0	49	PO_VDDCR_CPU0_SOC_VCCS	GND
PO_VCORE0_PWM2	2	PWM0	48	PO_VDDCR_CPU0_SOC_VCC	GND
PO_VCORE0_PWM3	3	PWM0	46	PO_VDDCR_CPU0_SOC_VINSEN	GND
PO_VCORE0_PWM4	4	PWM0	45	PO_VDDCR_CPU0_SOC_VINSEN	GND
PO_VCORE0_PWM5	5	PWM0	44	PO_VDDCR_CPU0_TEMP1	PO_VCORE0_TEMPORE 166
PO_VCORE0_PWM6	6	PWM0	43	PO_VDDCR_CPU0_TEMP2	PO_VCORE0_TEMPORE 167
PO_VCORE0_PWM7	7	PWM0	42	PO_VDDCR_CPU0_TEMP3	GND
PO_VCORE0_PWM8	8	PWM0	41	PO_VDDCR_CPU0_TEMP4	GND
PO_VCORE0_PWM9	9	PWM0	40	PO_VDDCR_CPU0_TEMP5	GND
PO_VCORE0_PWM10	10	PWM0	39	PO_VDDCR_CPU0_TEMP6	GND
PO_VCORE0_PWM11	11	PWM0	38	PO_VDDCR_CPU0_TEMP7	GND
PO_VCORE0_PWM12	12	PWM0	37	PO_VDDCR_CPU0_TEMP8	GND
PO_VDDCR_CPU0_SOC_PMSDA	13	PMSDA	36	PO_VDDCR_CPU0_TEMP9	GND
PO_VDDCR_CPU0_SOC_PMSCL	14	PMSCL	35	PO_VDDCR_CPU0_TEMP10	GND
PO_VDDCR_CPU0_SOC_PMSHRT	15	PMSHRT	34	PO_VDDCR_CPU0_TEMP11	GND
PO_VDDCR_CPU0_TEMP1	16	TEMP1	33	PO_VDDCR_CPU0_TEMP12	GND
PO_VDDCR_CPU0_TEMP2	17	TEMP2	32	PO_VDDCR_CPU0_TEMP13	GND
PO_VDDCR_CPU0_TEMP3	18	TEMP3	31	PO_VDDCR_CPU0_TEMP14	GND
PO_VDDCR_CPU0_TEMP4	19	TEMP4	30	PO_VDDCR_CPU0_TEMP15	GND
PO_VDDCR_CPU0_TEMP5	20	TEMP5	29	PO_VDDCR_CPU0_TEMP16	GND
PO_VDDCR_CPU0_TEMP6	21	TEMP6	28	PO_VDDCR_CPU0_TEMP17	GND
PO_VDDCR_CPU0_TEMP7	22	TEMP7	27	PO_VDDCR_CPU0_TEMP18	GND
PO_VDDCR_CPU0_TEMP8	23	TEMP8	26	PO_VDDCR_CPU0_TEMP19	GND
PO_VDDCR_CPU0_TEMP9	24	TEMP9	25	PO_VDDCR_CPU0_TEMP20	GND
PO_VDDCR_CPU0_TEMP10	25	TEMP10	24	PO_VDDCR_CPU0_TEMP21	GND
PO_VDDCR_CPU0_TEMP11	26	TEMP11	23	PO_VDDCR_CPU0_TEMP22	GND
PO_VDDCR_CPU0_TEMP12	27	TEMP12	22	PO_VDDCR_CPU0_TEMP23	GND
PO_VDDCR_CPU0_TEMP13	28	TEMP13	21	PO_VDDCR_CPU0_TEMP24	GND
PO_VDDCR_CPU0_TEMP14	29	TEMP14	20	PO_VDDCR_CPU0_TEMP25	GND
PO_VDDCR_CPU0_TEMP15	30	TEMP15	19	PO_VDDCR_CPU0_TEMP26	GND
PO_VDDCR_CPU0_TEMP16	31	TEMP16	18	PO_VDDCR_CPU0_TEMP27	GND
PO_VDDCR_CPU0_TEMP17	32	TEMP17	17	PO_VDDCR_CPU0_TEMP28	GND
PO_VDDCR_CPU0_TEMP18	33	TEMP18	16	PO_VDDCR_CPU0_TEMP29	GND
PO_VDDCR_CPU0_TEMP19	34	TEMP19	15	PO_VDDCR_CPU0_TEMP30	GND
PO_VDDCR_CPU0_TEMP20	35	TEMP20	14	PO_VDDCR_CPU0_TEMP31	GND
PO_VDDCR_CPU0_TEMP21	36	TEMP21	13	PO_VDDCR_CPU0_TEMP32	GND
PO_VDDCR_CPU0_TEMP22	37	TEMP22	12	PO_VDDCR_CPU0_TEMP33	GND
PO_VDDCR_CPU0_TEMP23	38	TEMP23	11	PO_VDDCR_CPU0_TEMP34	GND
PO_VDDCR_CPU0_TEMP24	39	TEMP24	10	PO_VDDCR_CPU0_TEMP35	GND
PO_VDDCR_CPU0_TEMP25	40	TEMP25	9	PO_VDDCR_CPU0_TEMP36	GND
PO_VDDCR_CPU0_TEMP26	41	TEMP26	8	PO_VDDCR_CPU0_TEMP37	GND
PO_VDDCR_CPU0_TEMP27	42	TEMP27	7	PO_VDDCR_CPU0_TEMP38	GND
PO_VDDCR_CPU0_TEMP28	43	TEMP28	6	PO_VDDCR_CPU0_TEMP39	GND
PO_VDDCR_CPU0_TEMP29	44	TEMP29	5	PO_VDDCR_CPU0_TEMP40	GND
PO_VDDCR_CPU0_TEMP30	45	TEMP30	4	PO_VDDCR_CPU0_TEMP41	GND
PO_VDDCR_CPU0_TEMP31	46	TEMP31	3	PO_VDDCR_CPU0_TEMP42	GND
PO_VDDCR_CPU0_TEMP32	47	TEMP32	2	PO_VDDCR_CPU0_TEMP43	GND
PO_VDDCR_CPU0_TEMP33	48	TEMP33	1	PO_VDDCR_CPU0_TEMP44	GND
PO_VDDCR_CPU0_TEMP34	49	TEMP34	0	PO_VDDCR_CPU0_TEMP45	GND



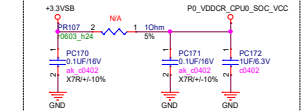
Reserved MOS
 VRHOT_Multi Function



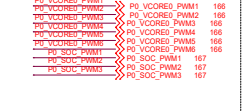
Enable
 VDDCR_CPU0



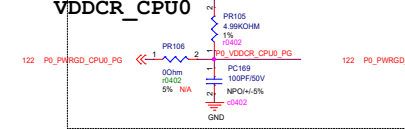
RAA229126 VCC



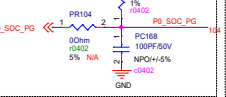
PWM



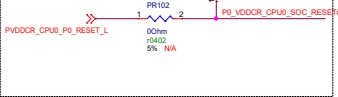
PGOOD
 VDDCR_CPU0



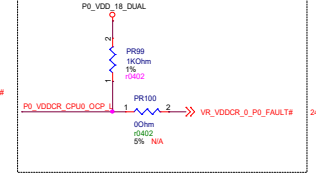
SOC
 CPU_SVI3_PWROK



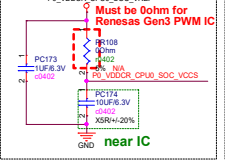
CVPU_SVI3_PWROK



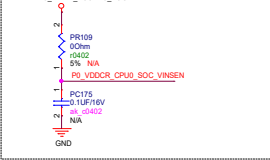
PVCC_Function



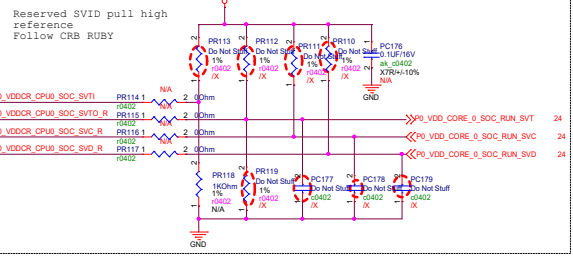
RAA229621 VCCS



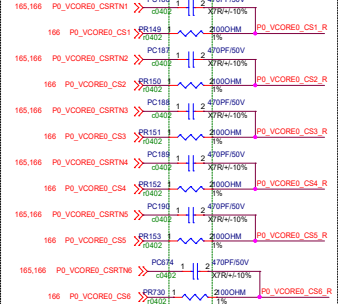
RAA229621 VINSEN



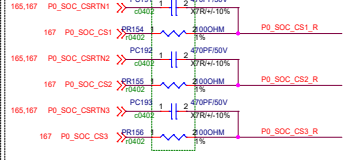
SVID BUS



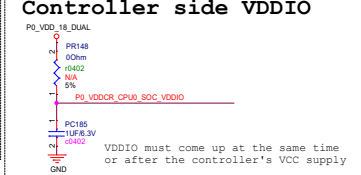
CURRENT SENSE near IC



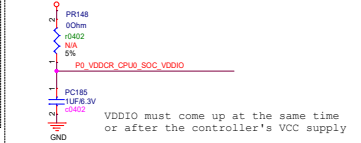
CURRENT SENSE near IC



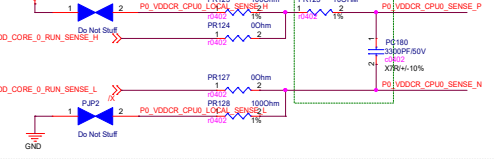
Current sense- SOC



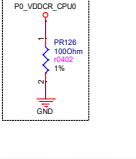
Controller side VDDIO



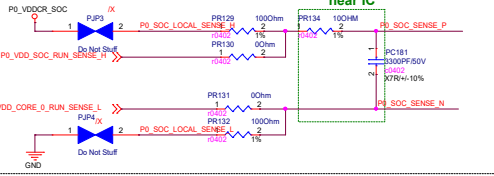
VSEN - VDDCR_CPU0



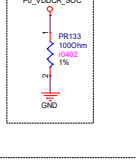
Dummy Load



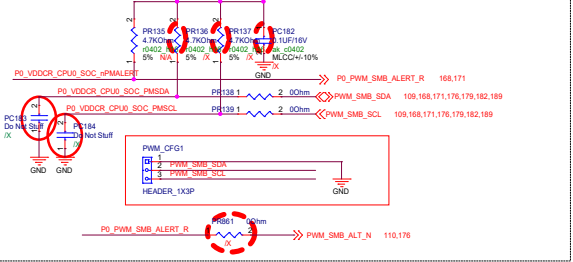
VSEN - SOC



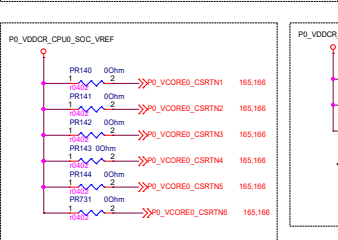
Dummy Load



PMBUS



Current sense- VDDCR_CPU0

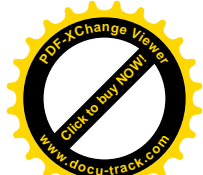


VREF-SOC

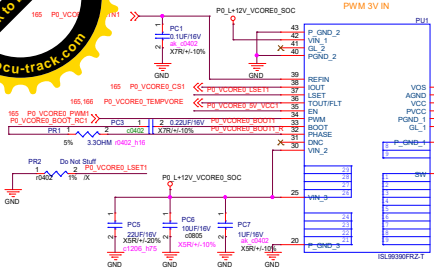


VREF-VDDCR_CPU0

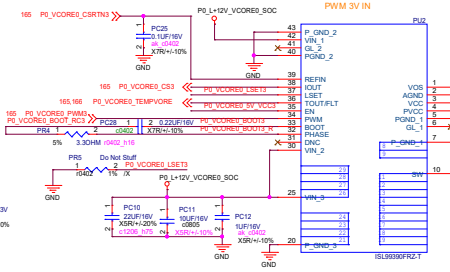




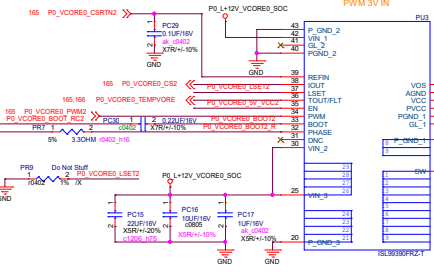
VDDCR_CPU0 PHASE1



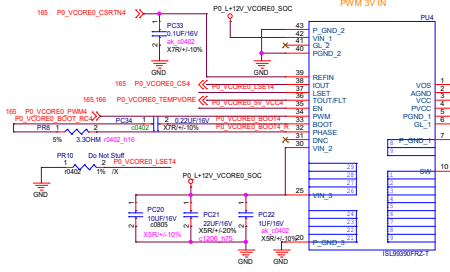
VDDCR_CPU0 PHASE3



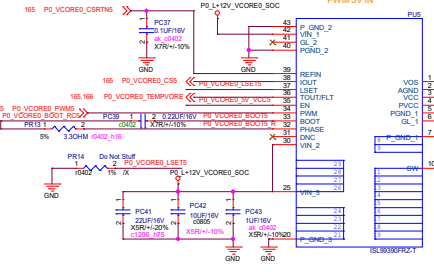
VDDCR_CPU0 PHASE2



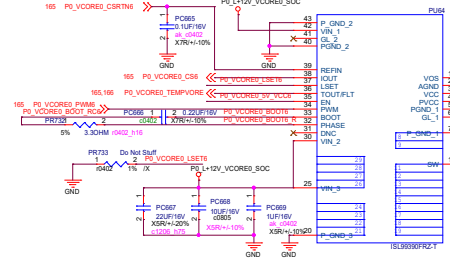
VDDCR_CPU0 PHASE4



VDDCR_CPU0 PHASE5

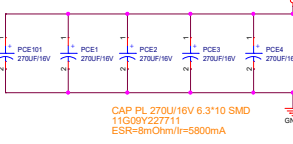


VDDCR_CPU0 PHASE6



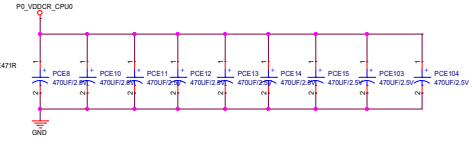
BDC = 0.17 mohm
I dc = 65A @ 4.5deg
I sat = 60A @ 8% load @ 25deg
M, D=7.62*7.49*4.96 mm

VDDCR_CPU0 SOC Input CAP

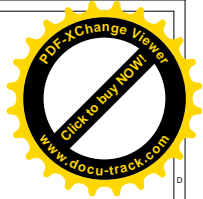
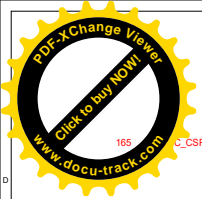


CAP PL 270U/16V 6.3*10 SMD
11G00Y227711
ESR=8mOhm/rl=5800nA

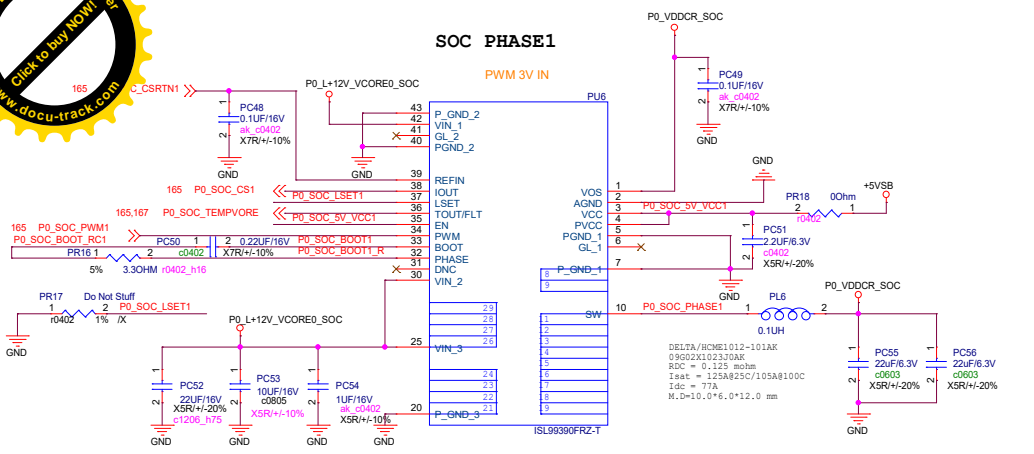
VDDCR_CPU0 Output CAP



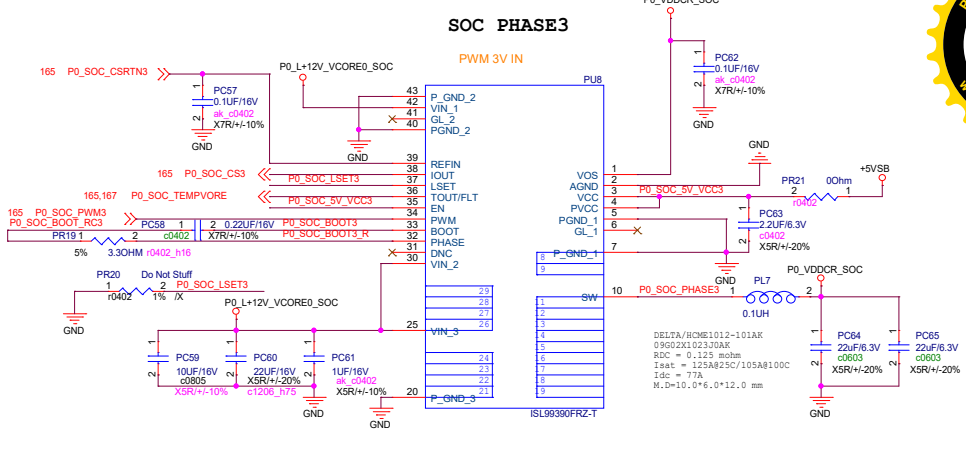
ASRock Rack
ASRock Rack
 Title : P0_CPU0_PHASE6
 Engineer: Ryan Lu
 Size Project Name
 Content GENOA2D24TW3-2L+ Rev
 Date: Monday, November 21, 2023 16:58
 Rev R1.0



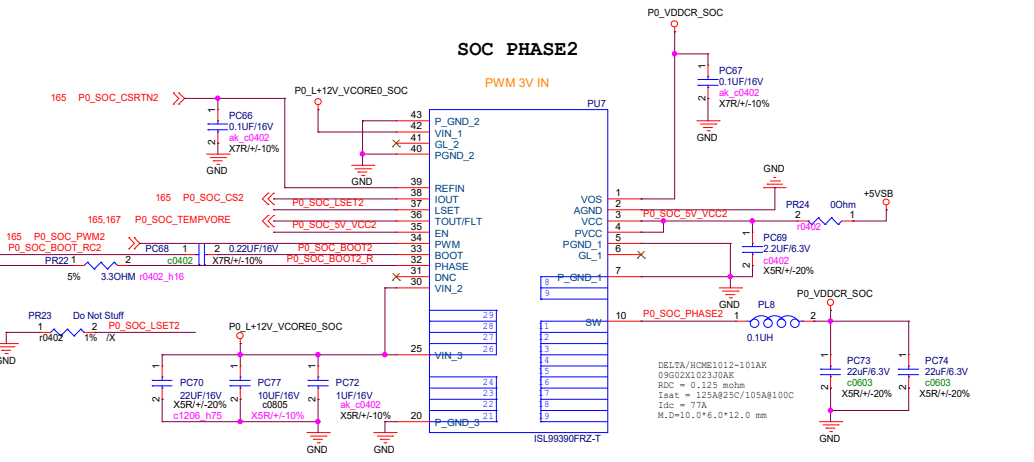
SOC PHASE1



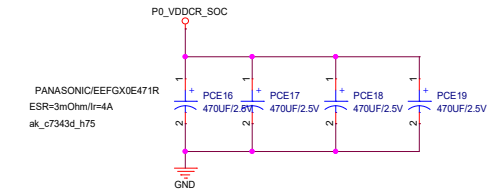
SOC PHASE3



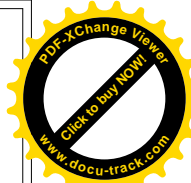
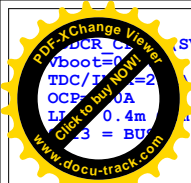
SOC PHASE2



SOC Output CAP



Title		
P0_SOC_PHASE13		
Size	Document Number	Rev
Custom	<Doc>	R1.0
Date:	Monday, November 21, 2022	Sheet 167 of 213



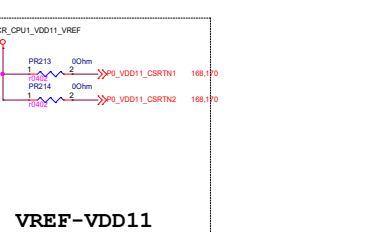
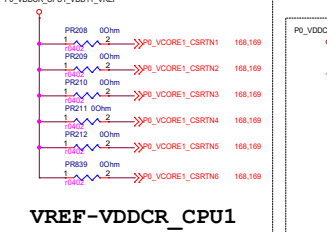
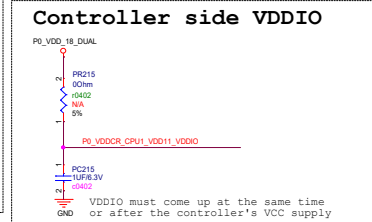
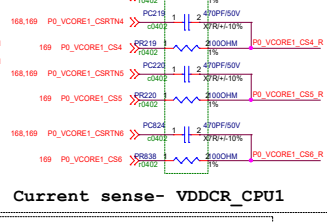
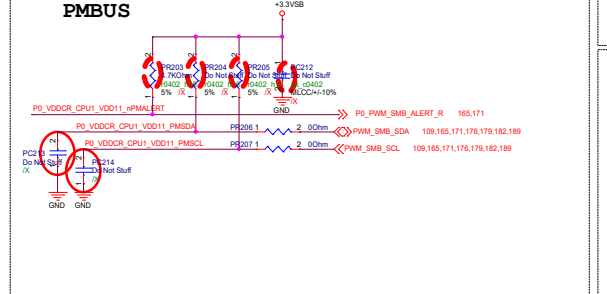
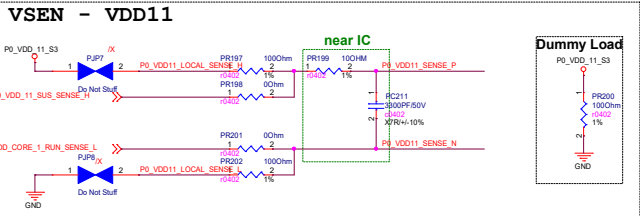
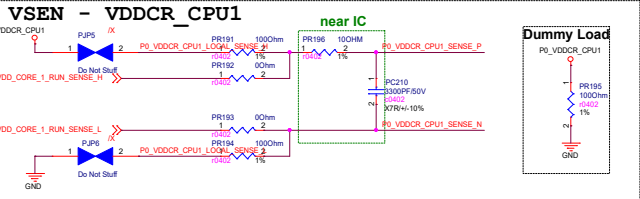
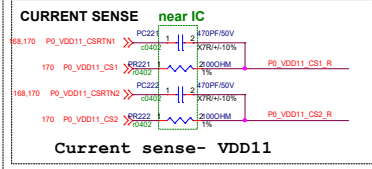
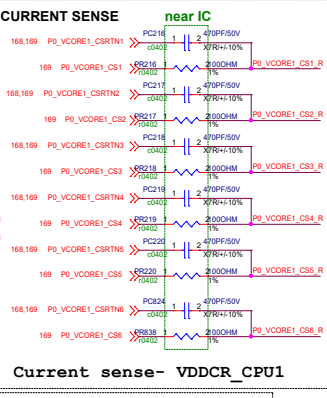
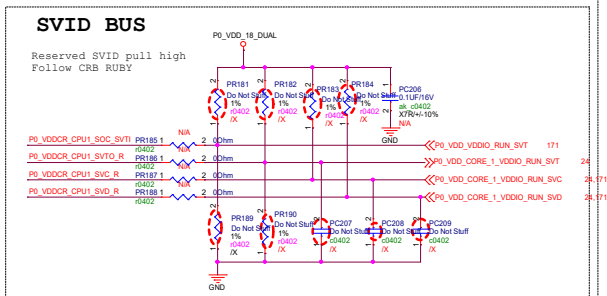
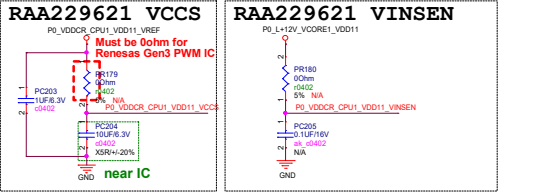
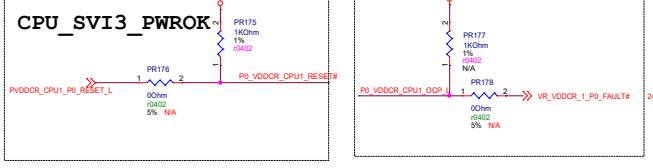
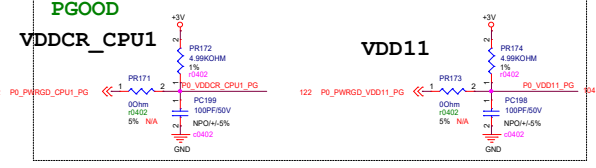
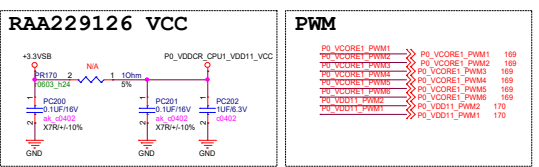
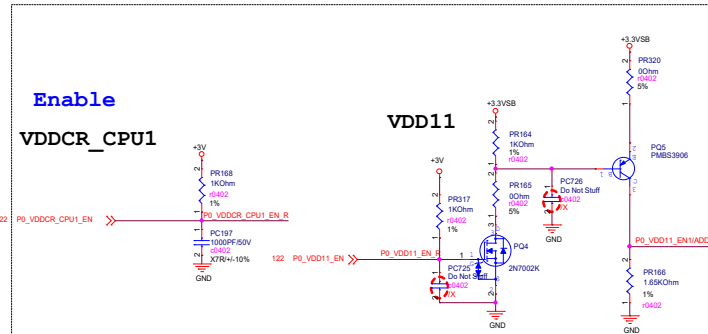
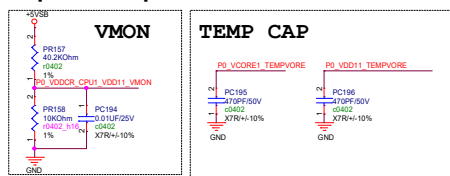
RAA229260 (SVI3)
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 TDC/IRMax=2/330A (IRM Ghigh)
 OCP=120A
 L=0.4mH
 I=3 = BU

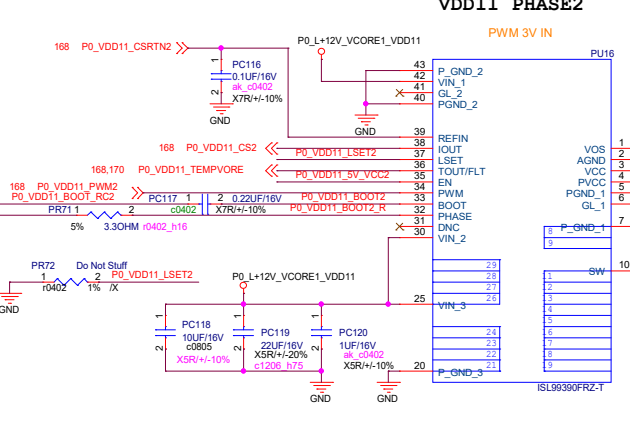
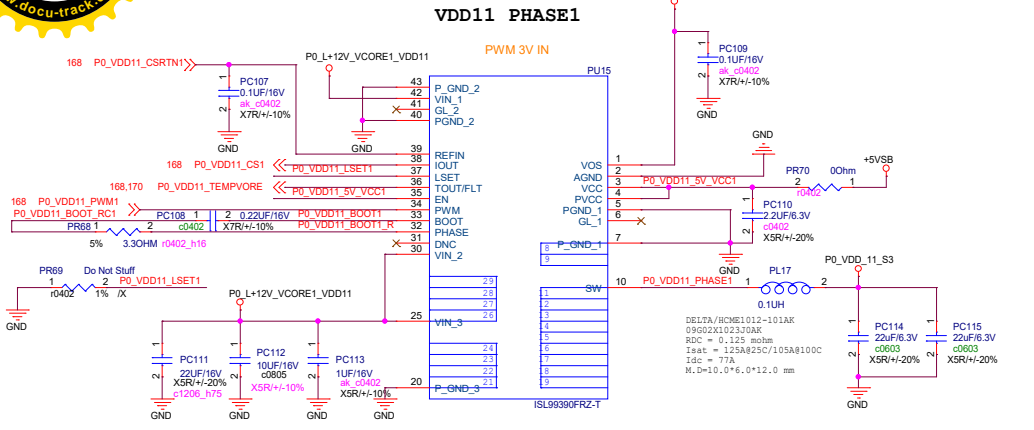
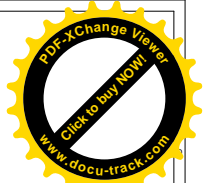
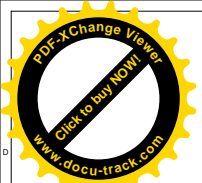
VDD11 (Non - SVI3)
 Vboot=1.1V
 TDC/IRMax=65A/80A
 OCP=120A

RAA229260 (SVI3)
 ISL PWM controller
 VDDCR_CPU1 + VDD11 = 6phase + 2phase
 PMBUS_ADDR = 62
 Config ID = 0

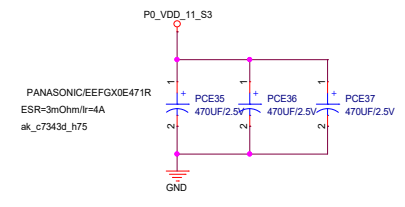
RAA229260 Part number change to 06G113204030AK
 Old part number had an address issue

PO_VCORE1_PWM1	1	PWM0	48	PO_VDDCR_CPU1_VDD11_VCCS	1	GND
PO_VCORE1_PWM2	2	PWM1	47	PO_VDDCR_CPU1_VDD11_VCC	2	VCCS
PO_VCORE1_PWM3	3	PWM2	46	PO_VDDCR_CPU1_VDD11_VINSEN	3	VINSEN
PO_VCORE1_PWM4	4	PWM3	45	PO_VDDCR_CPU1_VDD11_VMON	4	VMON
PO_VCORE1_PWM5	5	PWM4	44	PO_VDDCR_CPU1_VDD11_TEMP	5	TEMP
PO_VCORE1_PWM6	6	PWM5	43	PO_VDD11_TEMPVORE	6	PO_VCORE1_TEMPVORE 169
PO_VCORE1_PWM7	7	PWM6	42	PO_VDD11_TEMPVORE	7	PO_VDD11_TEMPVORE 170
PO_VCORE1_PWM8	8	PWM7	41	PO_VDDCR_CPU1_OCP_L	8	PO_VDDCR_CPU1_OCP_L
PO_VCORE1_PWM9	9	PWM8	40	PO_VDD11_SENSE_P	9	PO_VDD11_SENSE_P
PO_VCORE1_PWM10	10	PWM9	39	PO_VDD11_SENSE_N	10	PO_VDD11_SENSE_N
PO_VCORE1_PWM11	11	PWM10	38	PO_VDDCR_CST1_R	11	PO_VDDCR_CST1_R
PO_VDD11_PWM12	12	PWM11	37	PO_VDDCR_CST2_R	12	PO_VDDCR_CST2_R
PO_VDDCR_CPU1_PMSA	13	PMSA	36	PO_VCORE1_CS1_R	13	PO_VCORE1_CS1_R
PO_VDDCR_CPU1_PMSB	14	PMSB	35	PO_VCORE1_CS2_R	14	PO_VCORE1_CS2_R
PO_VDDCR_CPU1_PMSALERT	15	PMSALERT	34	PO_VCORE1_CS3_R	15	PO_VCORE1_CS3_R
PO_VDDCR_CPU1_PMSCL	16	PMSCL	33	PO_VCORE1_CS4_R	16	PO_VCORE1_CS4_R
PO_VDDCR_CPU1_EXTR	17	PSD	32	PO_VDD11_PMS1	17	PO_VDD11_PMS1
PO_VDDCR_CPU1_RESET#	18	ENI	31	PO_VDD11_PMS2	18	PO_VDD11_PMS2
PO_VDDCR_CPU1_VDDIO	19	RESET_L	30	PO_VDD11_PMS3	19	PO_VDD11_PMS3
PO_VDDCR_CPU1_SVID_R	20	SVID	29	PO_VDD11_PMS4	20	PO_VDD11_PMS4
PO_VDDCR_CPU1_SVID_R	21	SVID	28	PO_VDD11_PMS5	21	PO_VDD11_PMS5
PO_VDDCR_CPU1_SVID_R	22	SVID	27	PO_VDD11_PMS6	22	PO_VDD11_PMS6
PO_VDDCR_CPU1_SVID_R	23	SVID	26	PO_VDDCR_CPU1_SENSE_N	23	PO_VDD11_PMS7
PO_VDDCR_CPU1_SVID_R	24	SVID	25	PO_VDDCR_CPU1_SENSE_P	24	PO_VDD11_PMS8
PO_VDDCR_CPU1_SVID_R	25	SVID	24	PO_VDD11_PMS9	25	PO_VDD11_PMS9
PO_VDDCR_CPU1_SVID_R	26	SVID	23	PO_VDD11_PMS10	26	PO_VDD11_PMS10
PO_VDDCR_CPU1_SVID_R	27	SVID	22	PO_VDD11_PMS11	27	PO_VDD11_PMS11
PO_VDDCR_CPU1_SVID_R	28	SVID	21	PO_VDD11_PMS12	28	PO_VDD11_PMS12
PO_VDDCR_CPU1_SVID_R	29	SVID	20	PO_VDD11_PMS13	29	PO_VDD11_PMS13
PO_VDDCR_CPU1_SVID_R	30	SVID	19	PO_VDD11_PMS14	30	PO_VDD11_PMS14
PO_VDDCR_CPU1_SVID_R	31	SVID	18	PO_VDD11_PMS15	31	PO_VDD11_PMS15
PO_VDDCR_CPU1_SVID_R	32	SVID	17	PO_VDD11_PMS16	32	PO_VDD11_PMS16
PO_VDDCR_CPU1_SVID_R	33	SVID	16	PO_VDD11_PMS17	33	PO_VDD11_PMS17
PO_VDDCR_CPU1_SVID_R	34	SVID	15	PO_VDD11_PMS18	34	PO_VDD11_PMS18
PO_VDDCR_CPU1_SVID_R	35	SVID	14	PO_VDD11_PMS19	35	PO_VDD11_PMS19
PO_VDDCR_CPU1_SVID_R	36	SVID	13	PO_VDD11_PMS20	36	PO_VDD11_PMS20
PO_VDDCR_CPU1_SVID_R	37	SVID	12	PO_VDD11_PMS21	37	PO_VDD11_PMS21
PO_VDDCR_CPU1_SVID_R	38	SVID	11	PO_VDD11_PMS22	38	PO_VDD11_PMS22
PO_VDDCR_CPU1_SVID_R	39	SVID	10	PO_VDD11_PMS23	39	PO_VDD11_PMS23
PO_VDDCR_CPU1_SVID_R	40	SVID	9	PO_VDD11_PMS24	40	PO_VDD11_PMS24
PO_VDDCR_CPU1_SVID_R	41	SVID	8	PO_VDD11_PMS25	41	PO_VDD11_PMS25
PO_VDDCR_CPU1_SVID_R	42	SVID	7	PO_VDD11_PMS26	42	PO_VDD11_PMS26
PO_VDDCR_CPU1_SVID_R	43	SVID	6	PO_VDD11_PMS27	43	PO_VDD11_PMS27
PO_VDDCR_CPU1_SVID_R	44	SVID	5	PO_VDD11_PMS28	44	PO_VDD11_PMS28
PO_VDDCR_CPU1_SVID_R	45	SVID	4	PO_VDD11_PMS29	45	PO_VDD11_PMS29
PO_VDDCR_CPU1_SVID_R	46	SVID	3	PO_VDD11_PMS30	46	PO_VDD11_PMS30
PO_VDDCR_CPU1_SVID_R	47	SVID	2	PO_VDD11_PMS31	47	PO_VDD11_PMS31
PO_VDDCR_CPU1_SVID_R	48	SVID	1	PO_VDD11_PMS32	48	PO_VDD11_PMS32

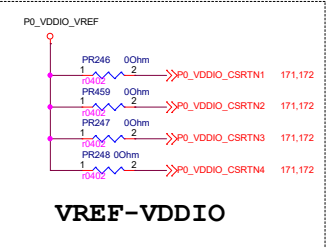
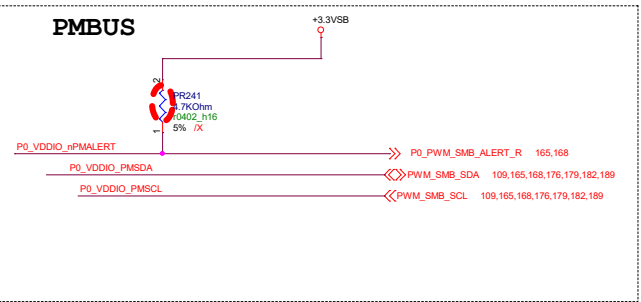
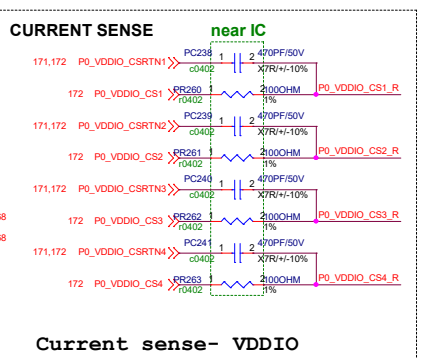
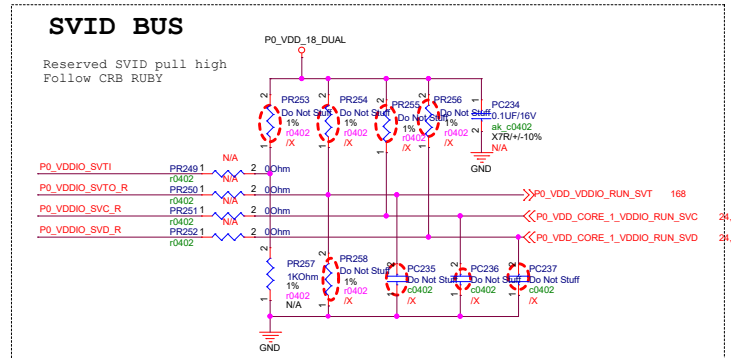
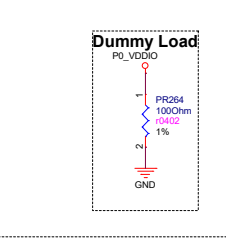
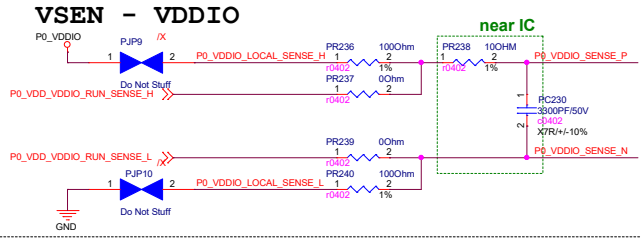
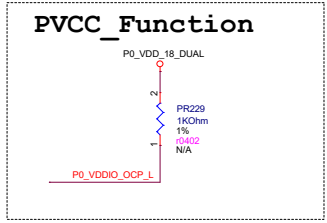
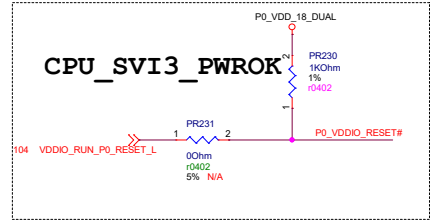
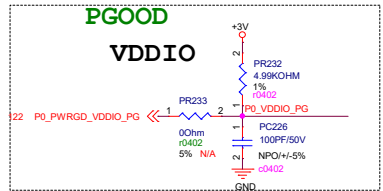
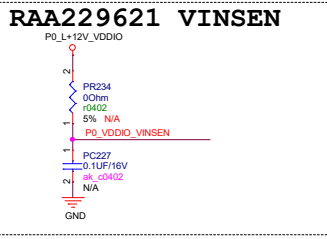
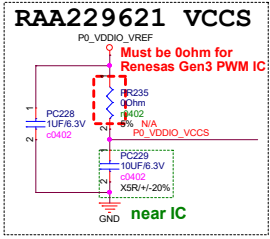
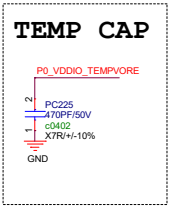
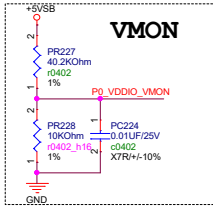
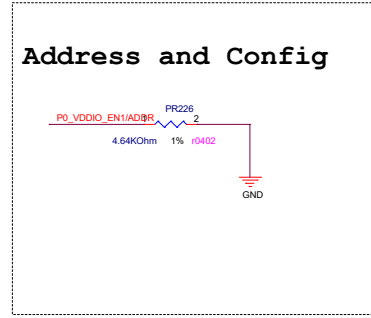
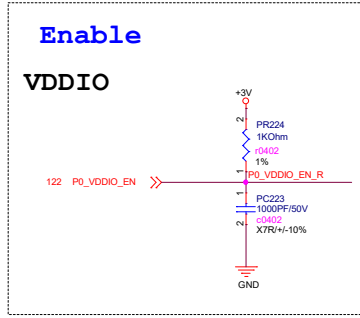
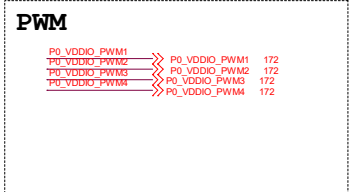
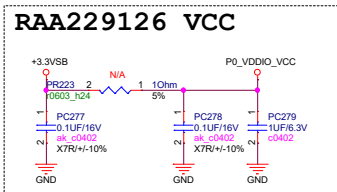
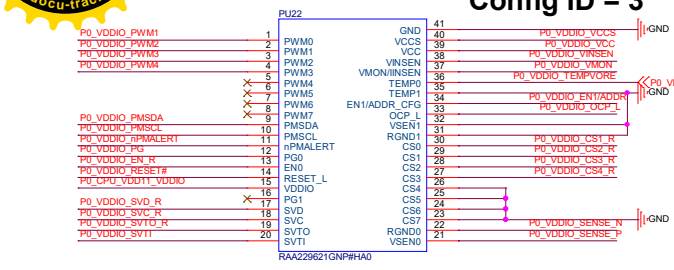
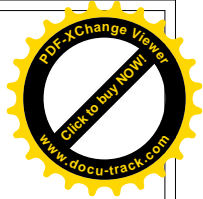
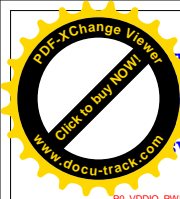


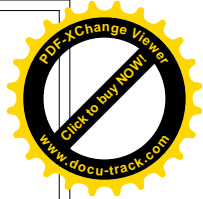
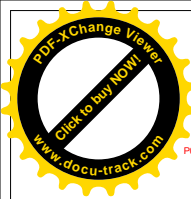


VDD11 Output CAP

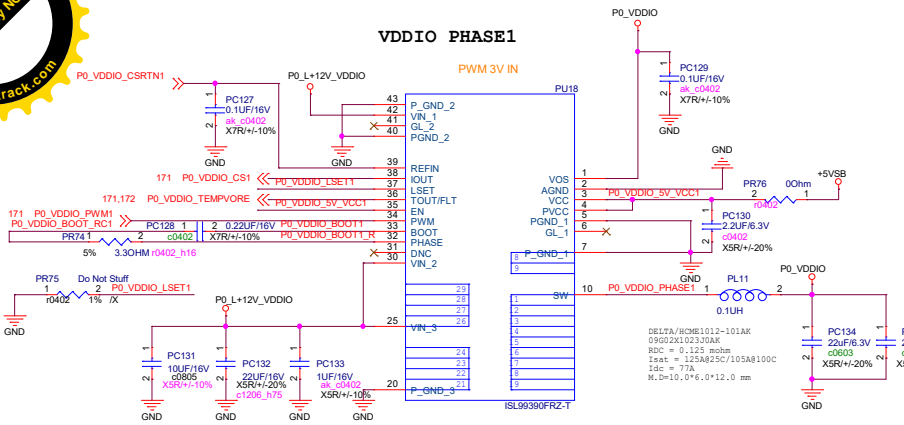


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P0_VDD11_PHASE12		
Size	Document Number	Rev
Custom<Doc>		R1.0
Date:	Monday, November 21, 2022	Sheet 170 of 213

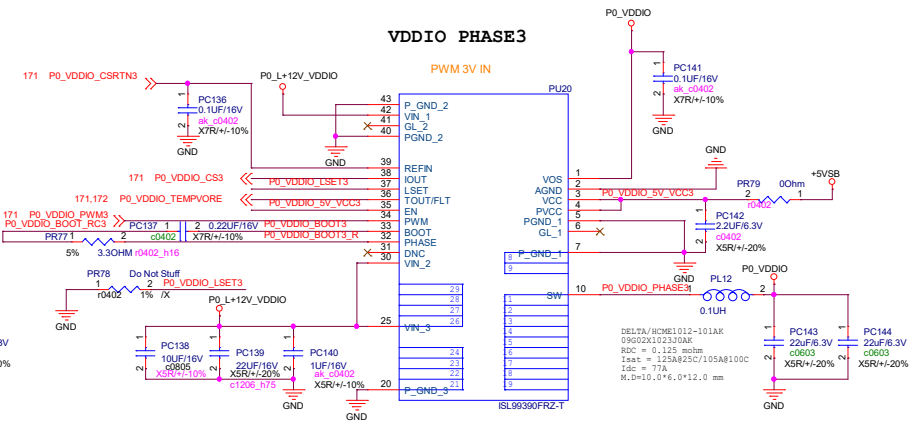




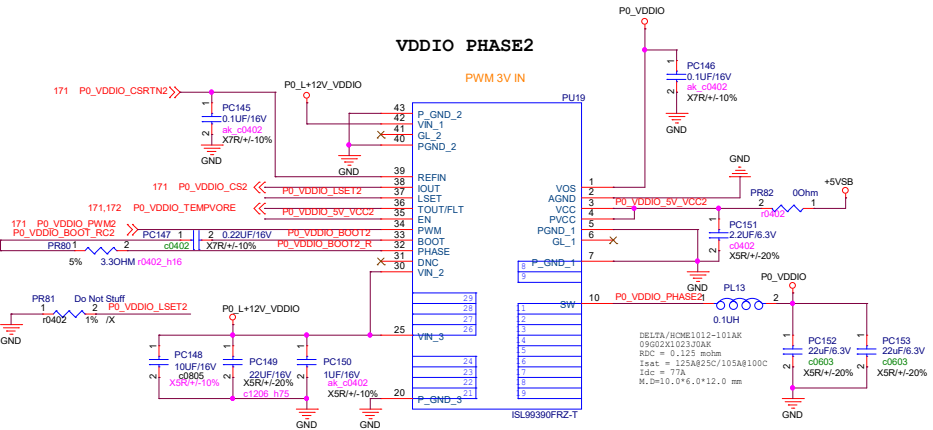
VDDIO PHASE1



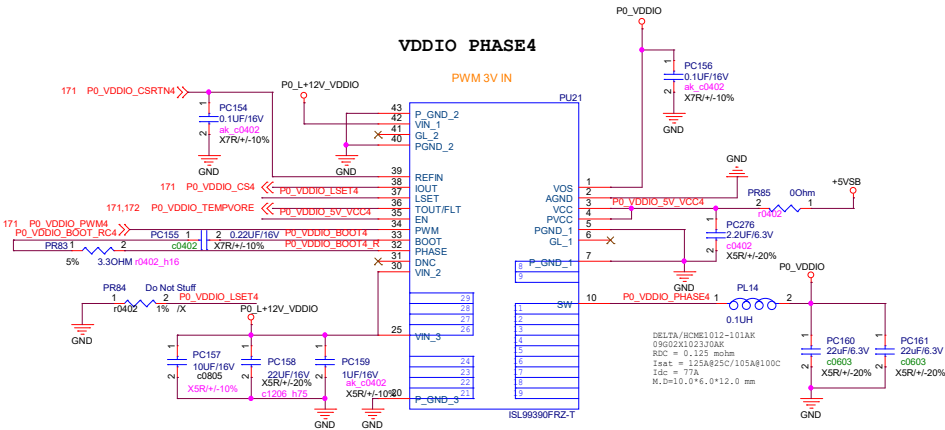
VDDIO PHASE3



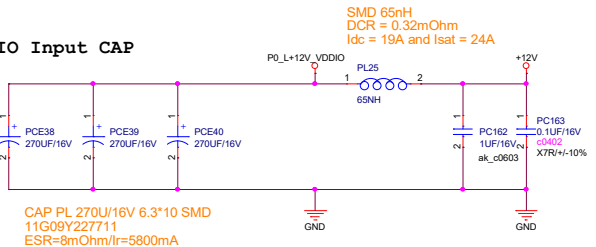
VDDIO PHASE2



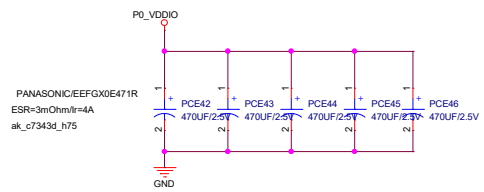
VDDIO PHASE4



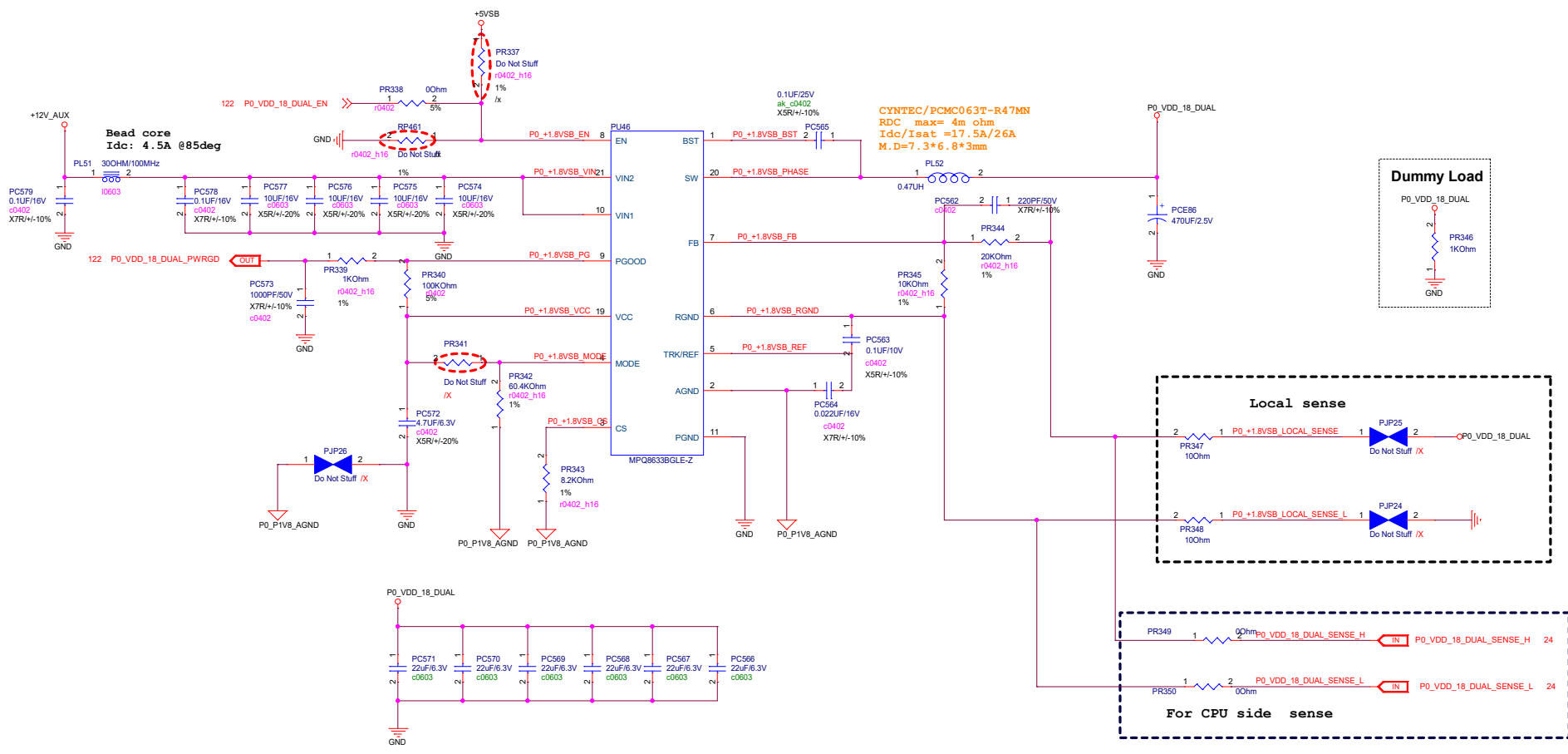
VDDIO Input CAP



VDDIO Output CAP

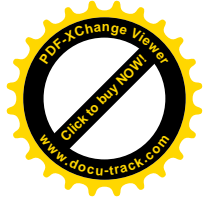
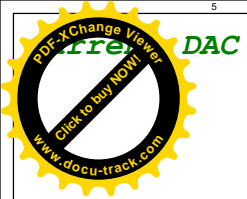


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Size	Document Number			
Customer	Doc			
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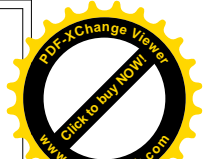
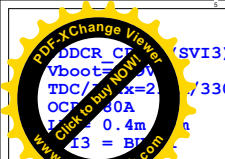
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ASRock Rack		Title : 086_VDDCR_CPU_IR35201	
ASRock Rack		Engineer: <i>Ryan Lu</i>	
Size: Custom	Project Name: GENOA2D24TM3-2L+	Rev: R1.01	
Date: Monday, November 21, 2022	ISheet: 174	of	213



<Variant Name>

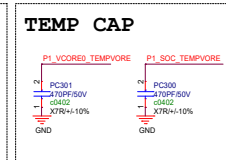
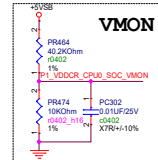
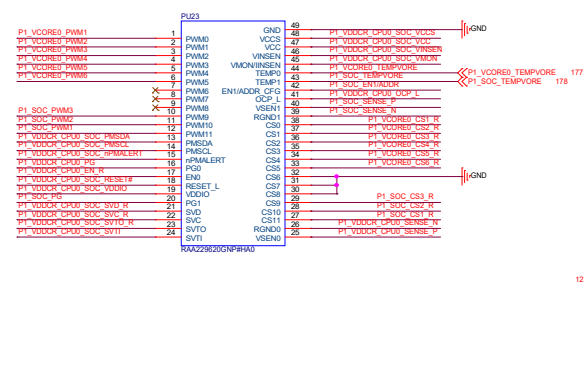
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Size	Project Name	Rev	
Custom	GENOA2D24TM3-2L+	R1.0	
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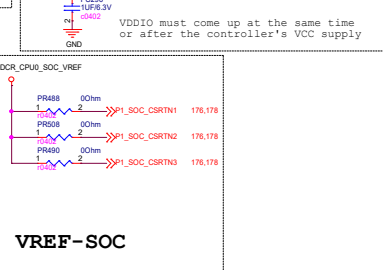
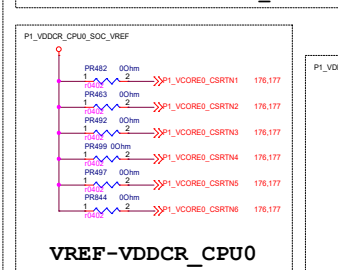
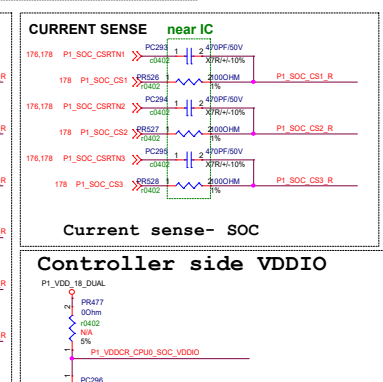
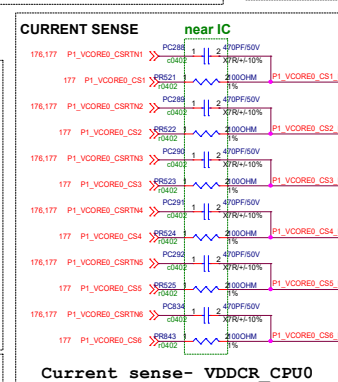
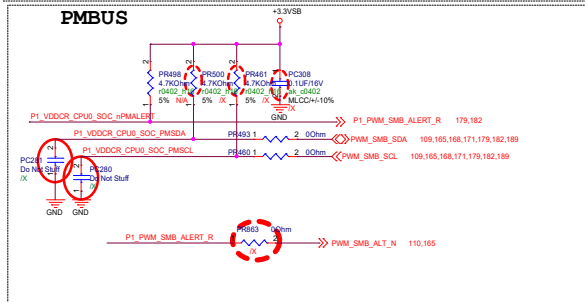
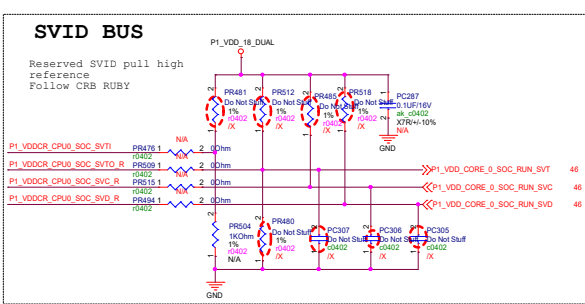
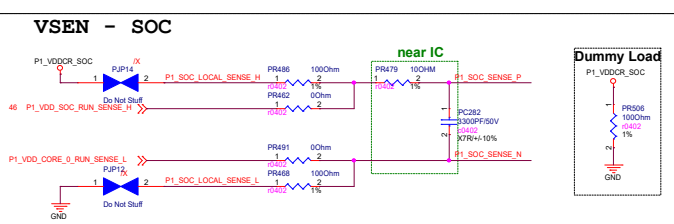
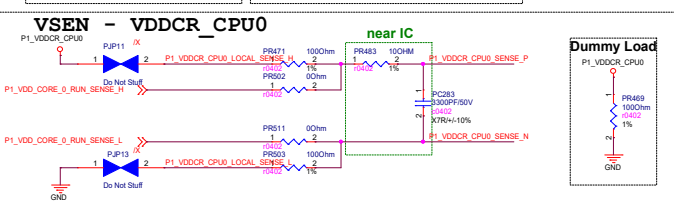
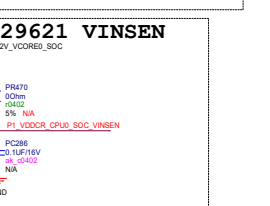
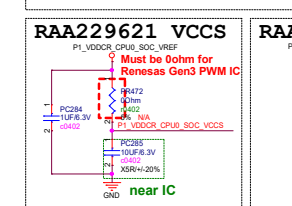
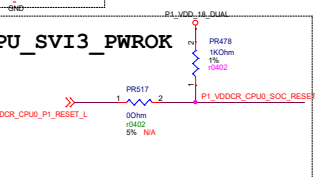
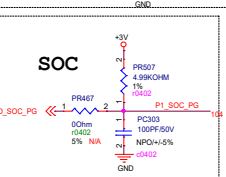
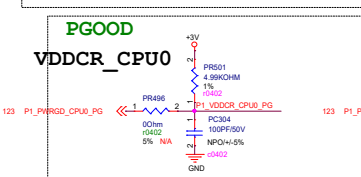
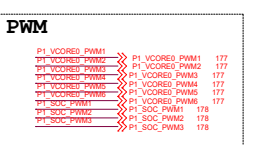
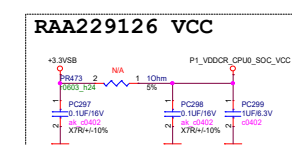
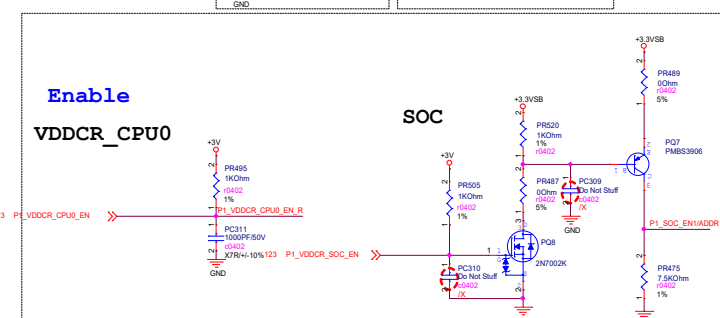
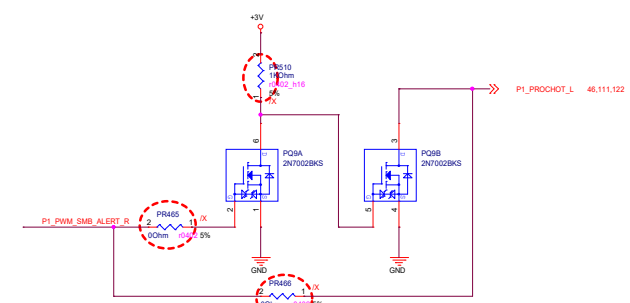
VDDCR_CPU0 (SVI3)
 Vboot=0.9V
 TDC/IMax=105A/130A (IRM Ghigh)
 OCP=170A
 SVI3 = BUS#1

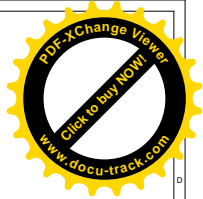
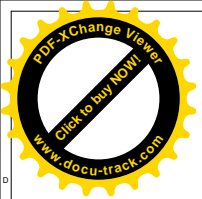
RAA229260 (SVI3)
 ISL PWM controller
 VDDCR_CPU0 + SOC = 6phase + 3phase
 PMBUS ADDR = 72
 Config ID = 3

Part number change to 06G113204030AK
 Old part number had an address issue

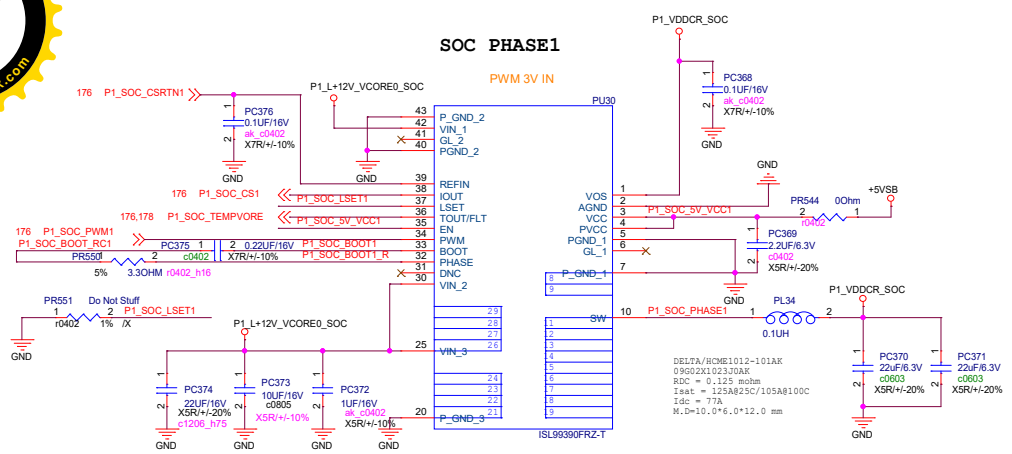


Reserved MOS
 VRHOT_Multi Function

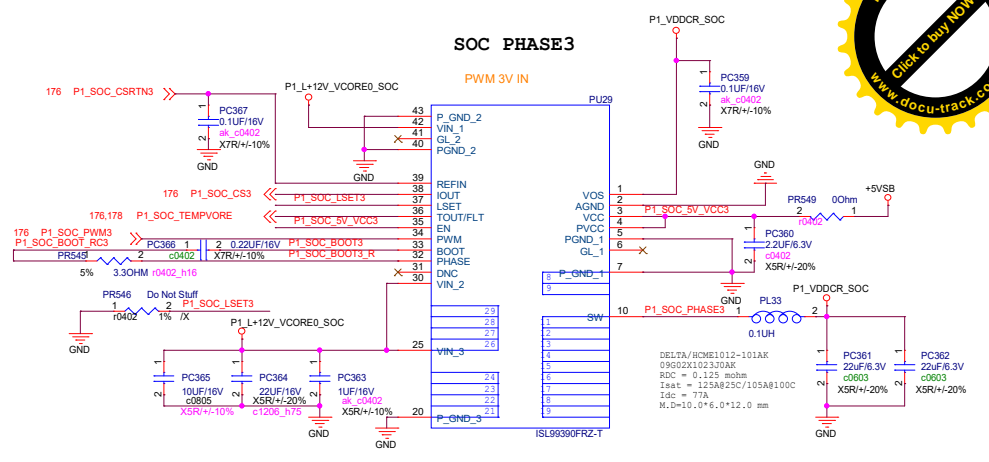




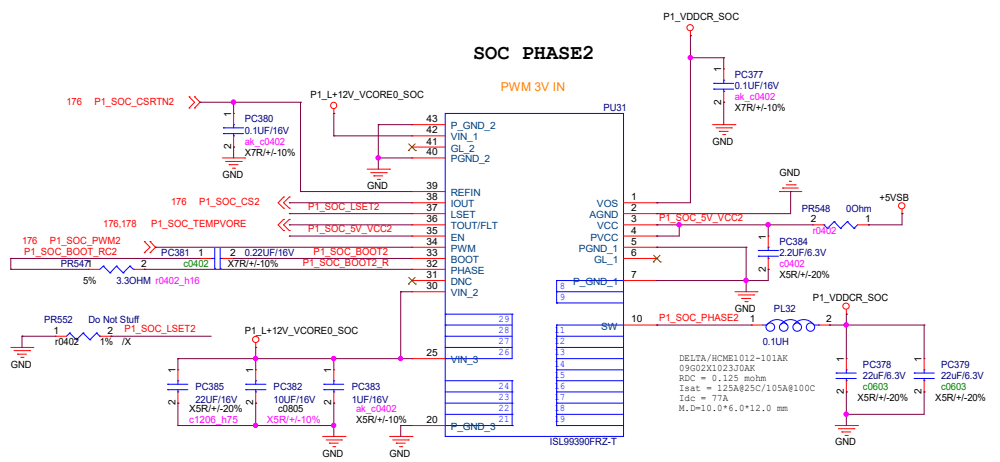
SOC PHASE1



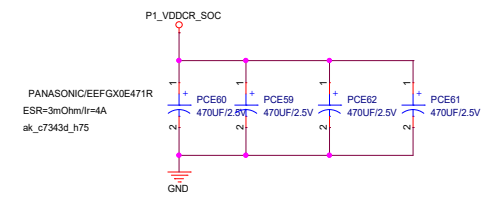
SOC PHASE3



SOC PHASE2

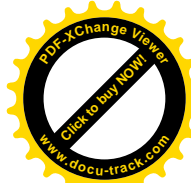
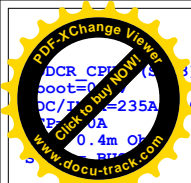


SOC Output CAP



<Variant Name>

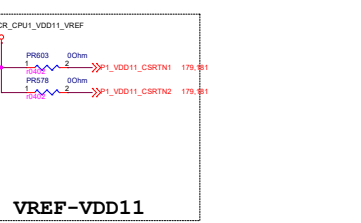
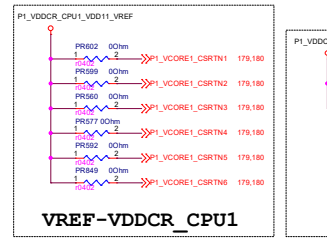
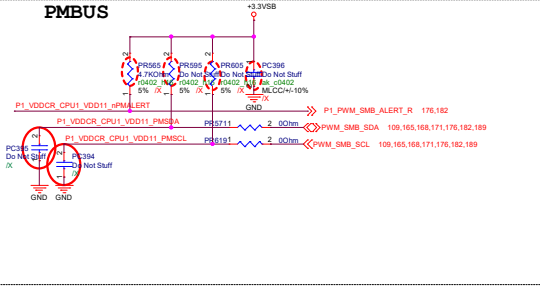
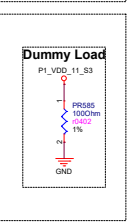
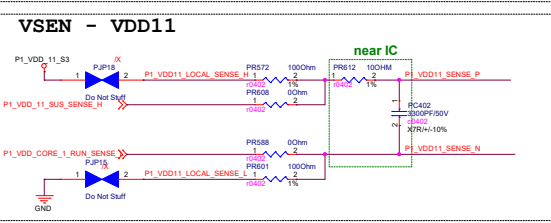
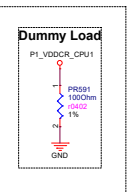
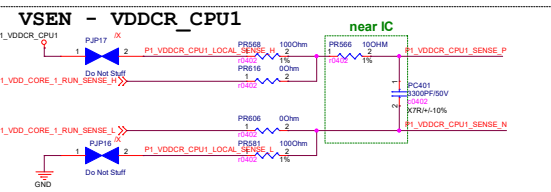
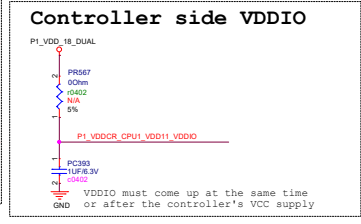
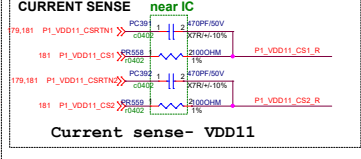
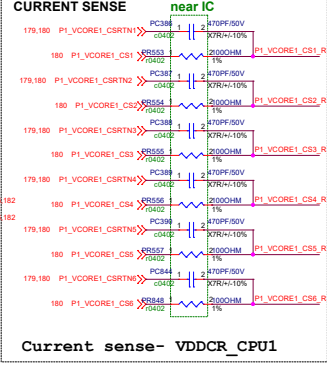
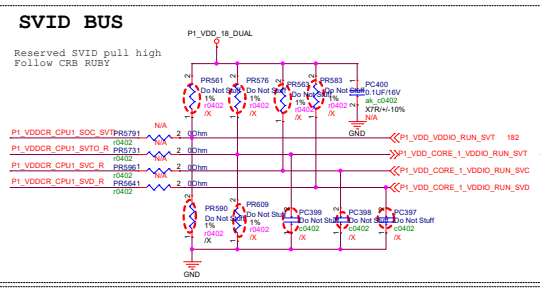
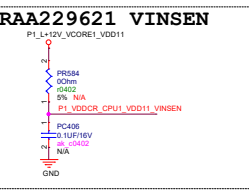
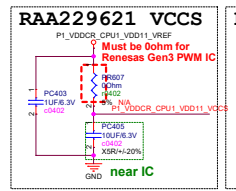
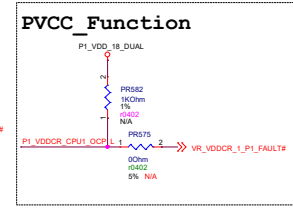
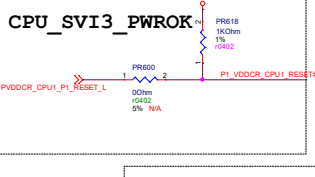
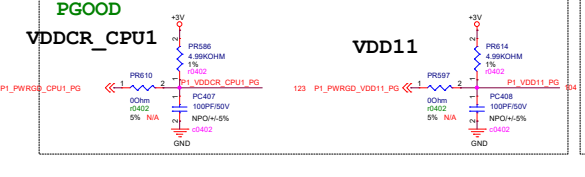
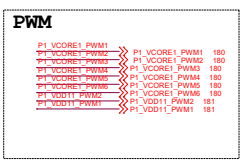
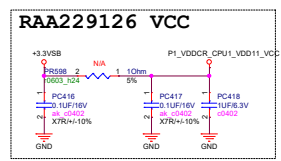
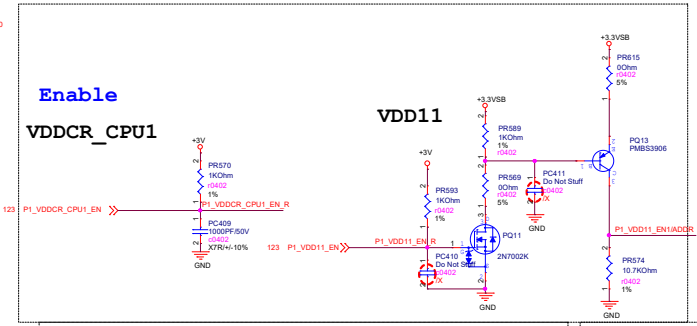
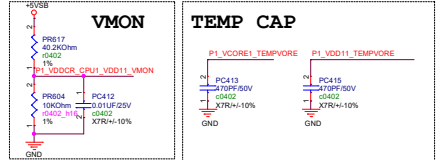
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ASRock Rack		Engineer: Ryan Lu	
Size	Project Name	Rev	
Custom	GENOA2D24TM3-2L+	R1.0	
Date: Monday, November 21, 2022	Sheet	178	of 213

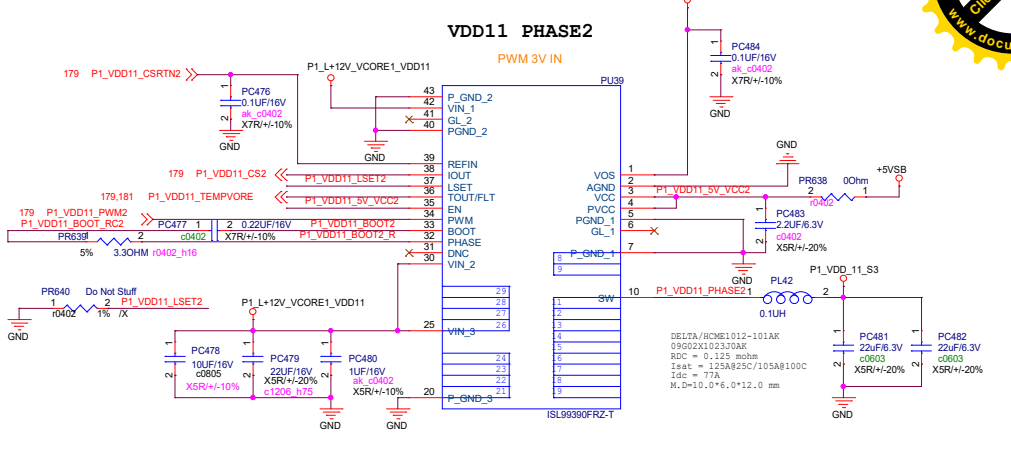
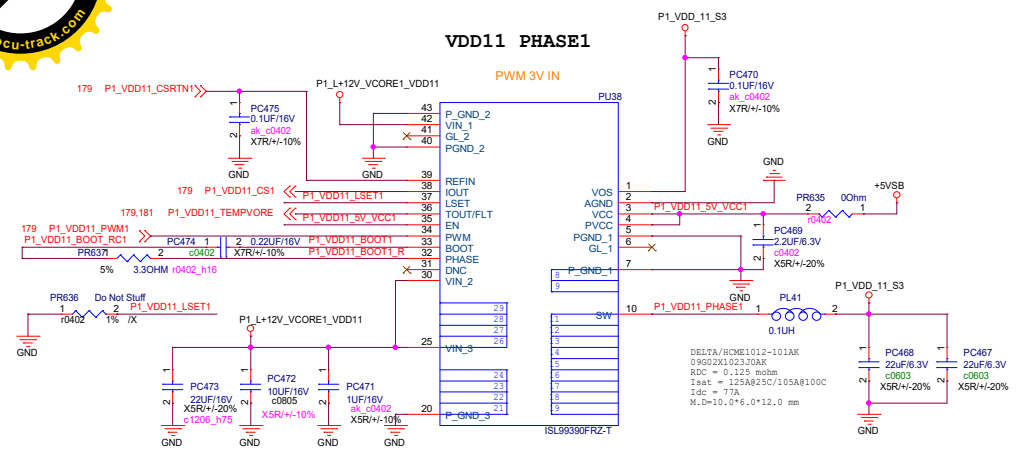
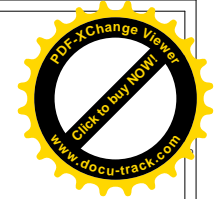
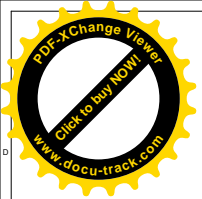


RAA229260 (SVI3)
 ISL PWM controller
 VDDCR_CP1 + VDD11 = 6phase + 2phase
 Vboot=1.1V
 TDC/Imax=65A/80A
 PMBUS_ADDR = 74
 Config ID = 2

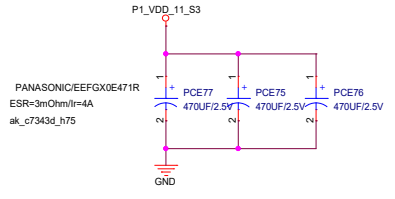
RAA229260 Part number change to 06G113204030AK
 Old part number had an address issue

PI_VCORE1_PWM1	PWM1	48	PI_VDDCR_CPU1_VDD11_VCC5	GND
PI_VCORE1_PWM2	PWM2	49	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VCORE1_PWM3	PWM3	50	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VCORE1_PWM4	PWM4	51	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VCORE1_PWM5	PWM5	52	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VCORE1_PWM6	PWM6	53	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM2	PWM2	49	PI_VDDCR_CPU1_VDD11_VCC5	GND
PI_VDD11_PWM3	PWM3	50	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM4	PWM4	51	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM5	PWM5	52	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM6	PWM6	53	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM7	PWM7	54	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM8	PWM8	55	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM9	PWM9	56	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM10	PWM10	57	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM11	PWM11	58	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM12	PWM12	59	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM13	PWM13	60	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM14	PWM14	61	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM15	PWM15	62	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM16	PWM16	63	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM17	PWM17	64	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM18	PWM18	65	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM19	PWM19	66	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM20	PWM20	67	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM21	PWM21	68	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM22	PWM22	69	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM23	PWM23	70	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM24	PWM24	71	PI_VDDCR_CPU1_VDD11_VCC	GND
PI_VDD11_PWM25	PWM25	72	PI_VDDCR_CPU1_VDD11_VCC	GND



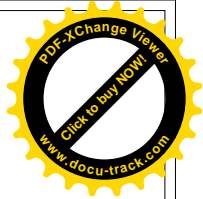
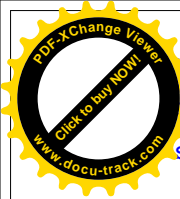


VDD11 Output CAP



<Variant Name>

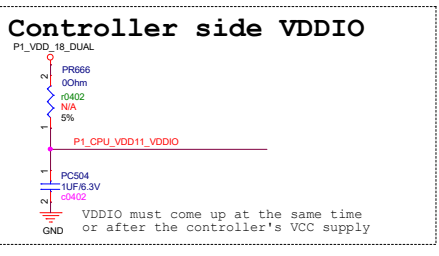
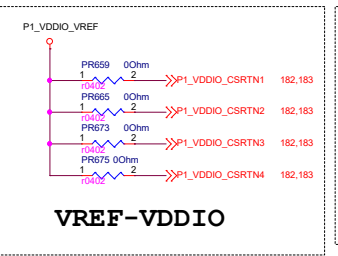
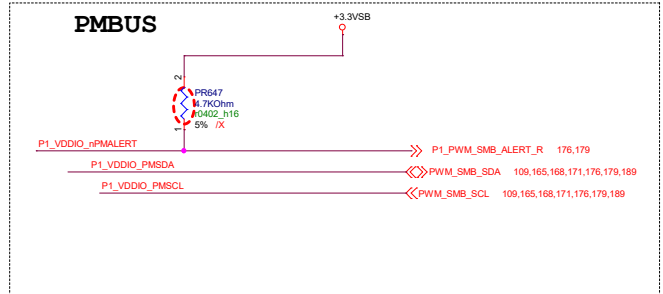
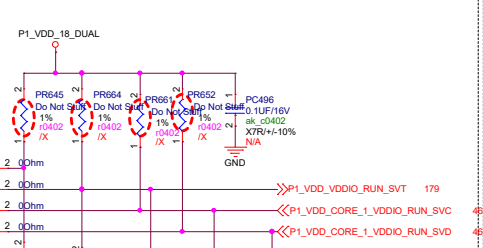
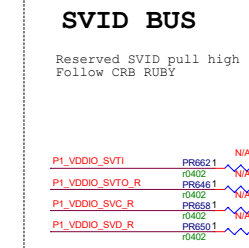
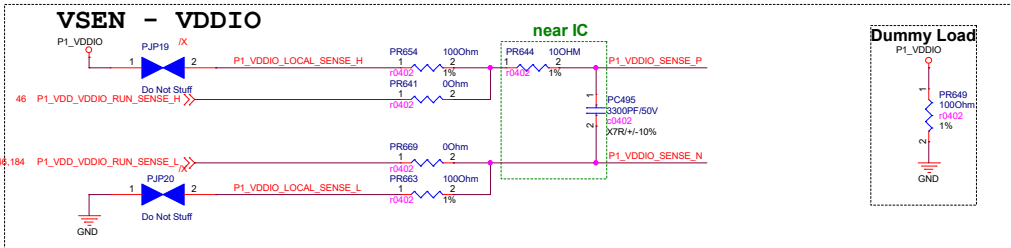
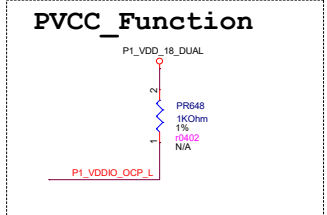
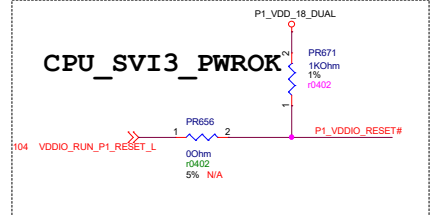
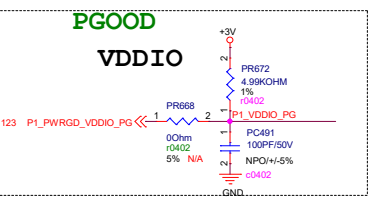
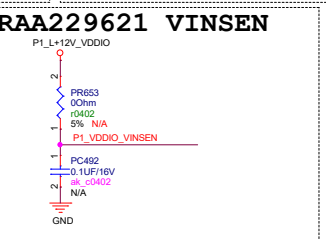
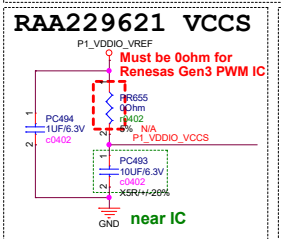
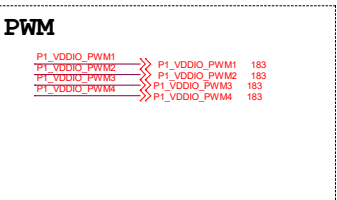
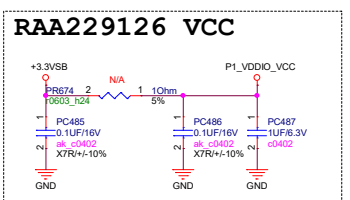
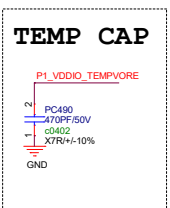
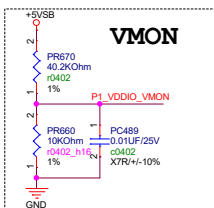
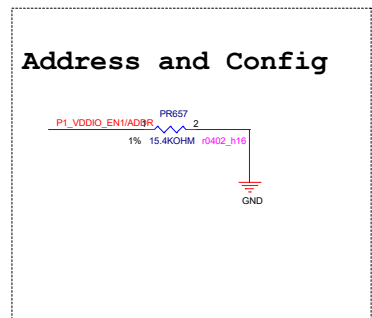
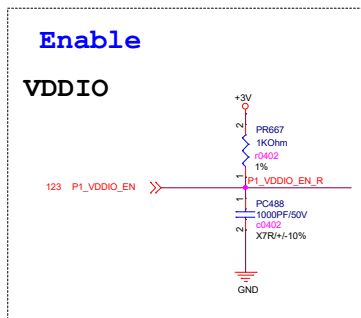
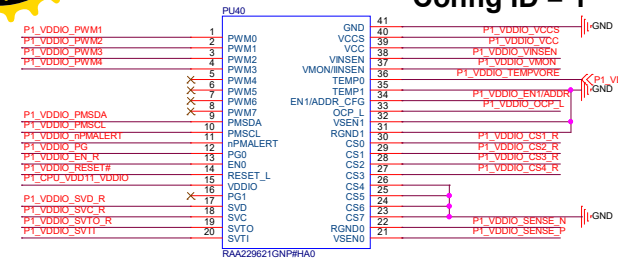
ASRock Rack		Title : P1_VDD11_PHASE12	
ASRock Rack		Engineer: Ryan Lu	
Size	Project Name	Rev	
Chartoon	GENOA2D24TM3-2L+	R1.01	
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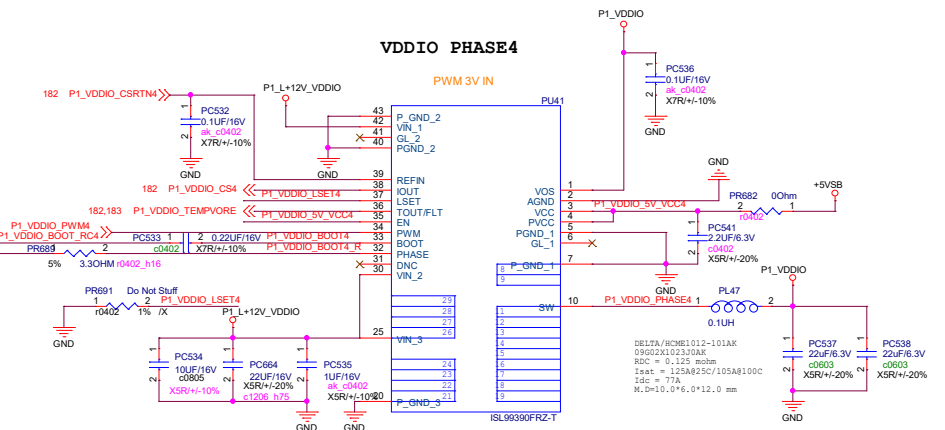
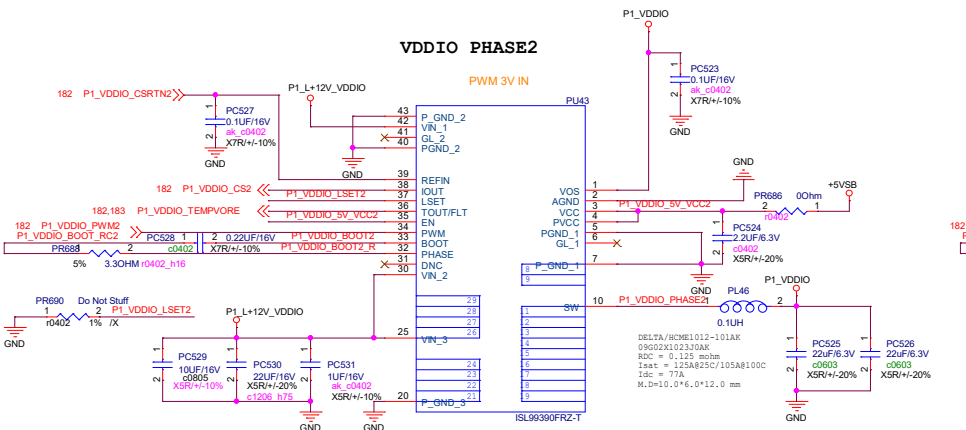
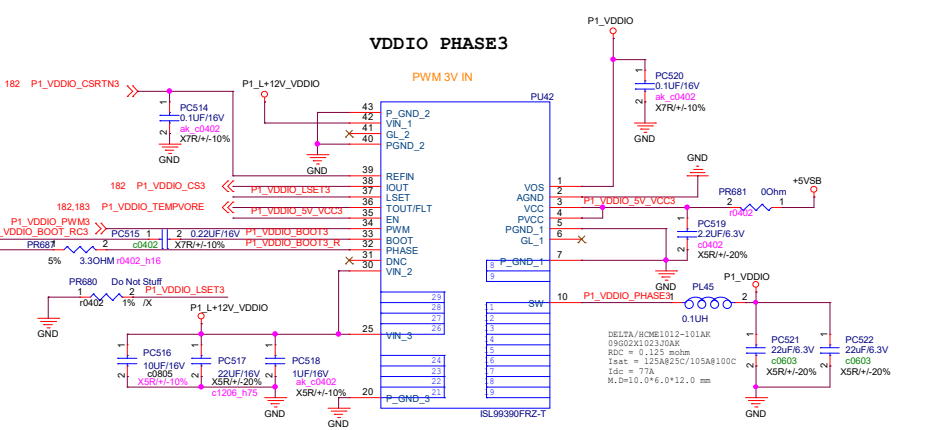
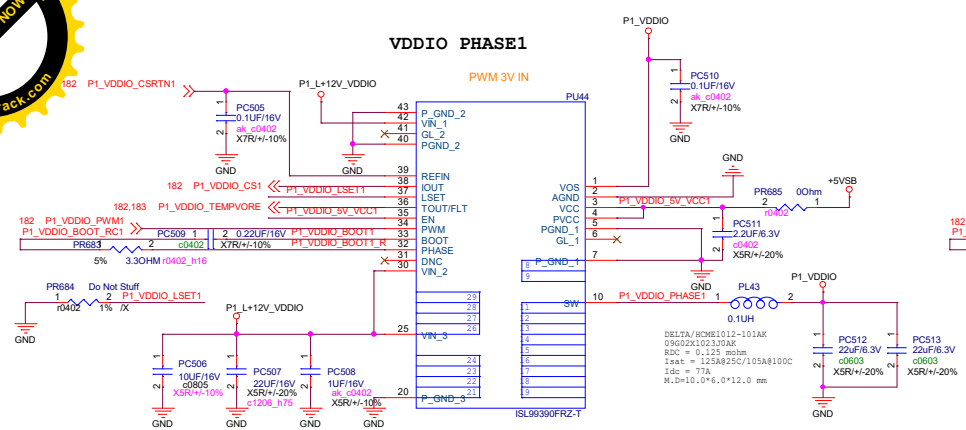
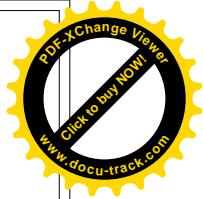
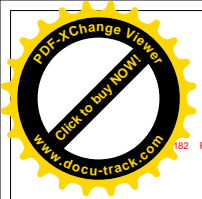


VDDIO (SVI3)
 Boot=1.1V
 DC/IMax=120A/140A
 CP=185A
 SVI3 = BUS#2

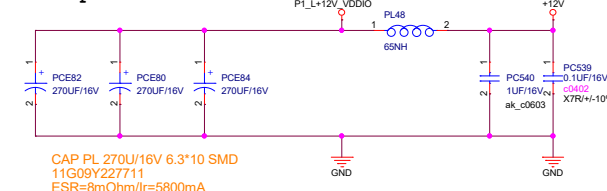
RAA229261 (SVI3)
 ISL PWM controller
 VDDIO = 4Phase
 PMBUS ADDR = 75
 Config ID = 1

RAA229261 Part number change to 06G113205040AK
 Old part number had an address issue

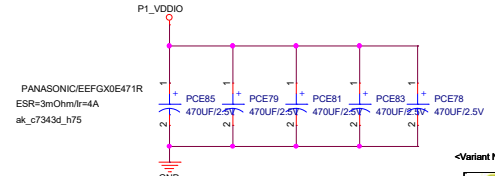


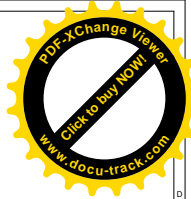
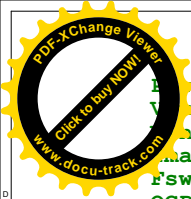


VDDIO Input CAP

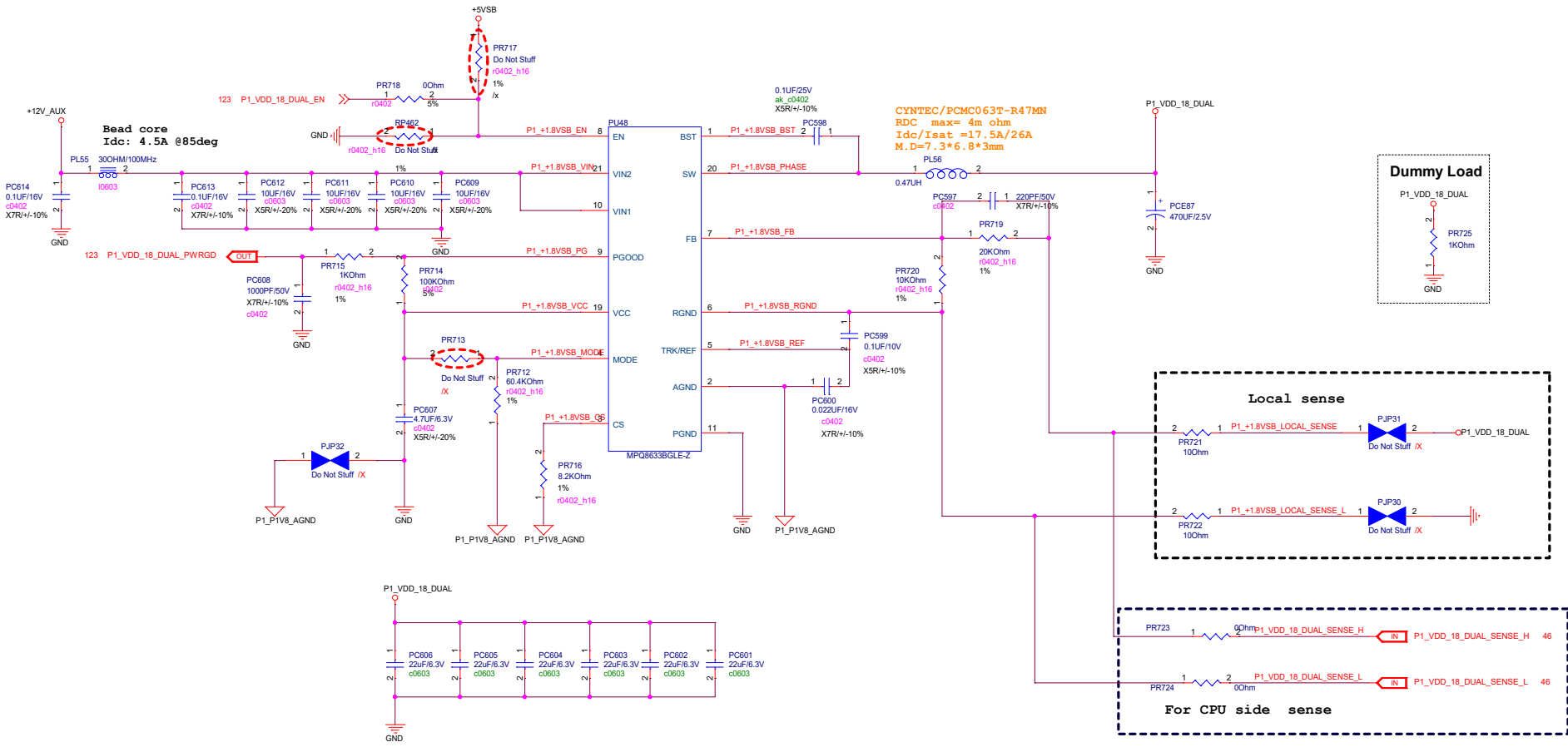


VDDIO Output CAP



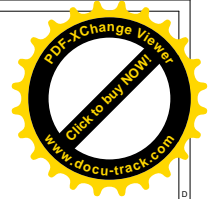
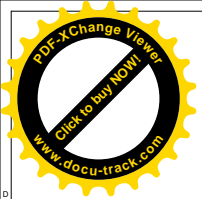


Power Rail : P0_VDD_18_DUAL
 Voltage : +1.8V
 Current : +12V +5VSB_DUAL
 I_max : 11A (contain VDDIO_AUDDIO)
 f_sw : 1000KHz
 OCP : 15.2A
 soft_star : 2ms




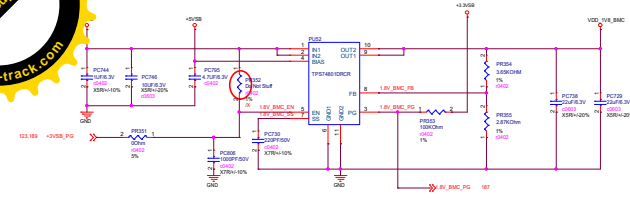
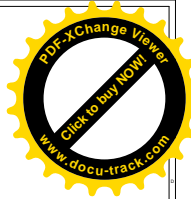
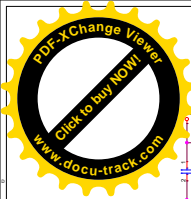
<Variant Name>

ASRock Rack		Title : 082_VCCM_ABCD IR35201	
ASRock Rack		Engineer: <i>Ryan Lu</i>	
Size	Project Name	GENOA2D24TM3-2L+	Rev R1.0
Custom	Date: Monday, November 21, 2022	Sheet 185 of 213	

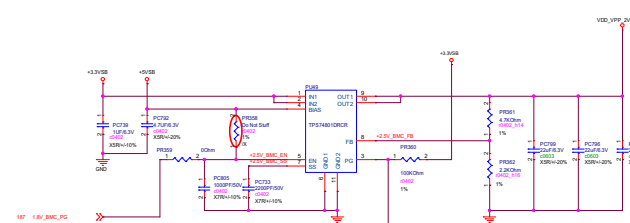


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		Title : <Title>	
<i>ASRock Rack</i>		Engineer: <i>Ryan Lu</i>	
Size Custom	Project Name GENOA2D24TM3-2L+	Rev R1.01	
Date: <i>Monday, November 21, 2022</i>	Sheet	186	of 213

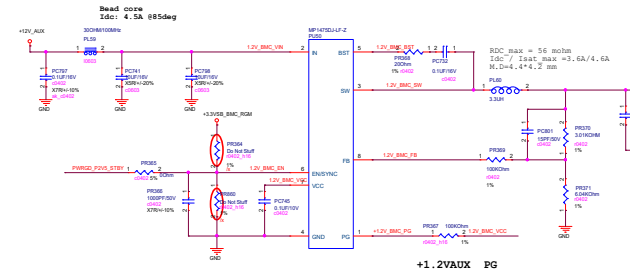


Power Rail : +1.8V_BMC_AUX
 I_{dc} : 0.086A
 F_{sw} : 2.5MHz
 OCP : 3A

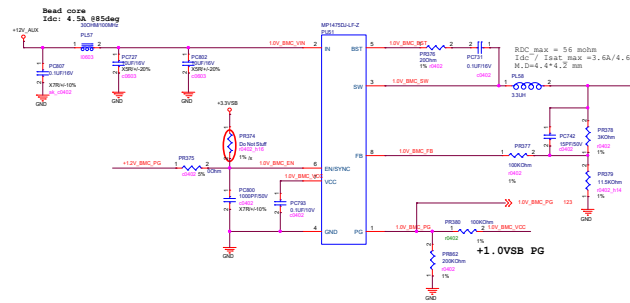


power rail: P2V5_STBY
 Vout: +2.5V
 Vin: +3.3VSB
 Imax : 0.1A(BMC)
 OCP : 2~5.5A
 SoftStart : 4ms

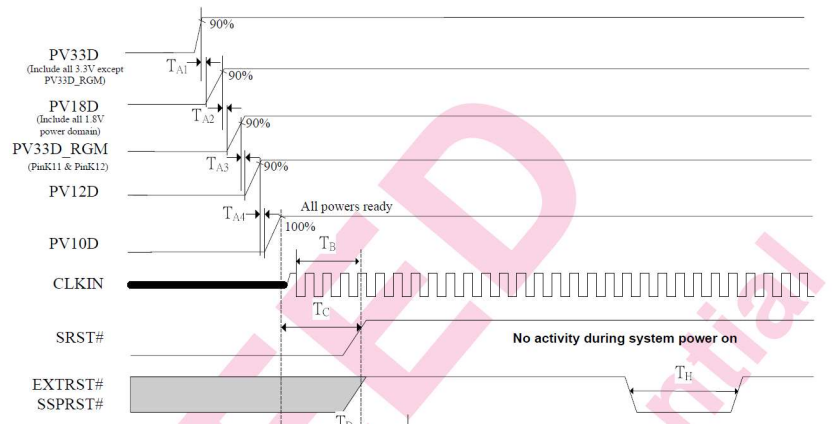
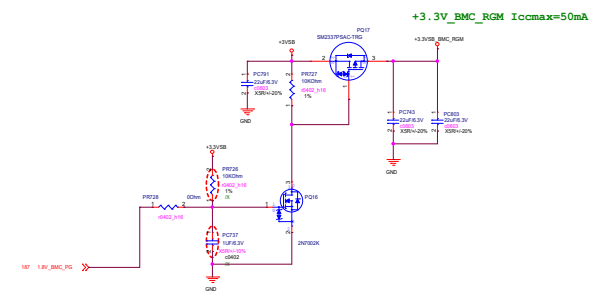
$V_{out} = 0.8 * (1 + 4.7 / 2.2) = 2.509V$



power rail: P1V2_STBY
 Vout: +1.2V
 Vin: +12V +5VSB_DUAL
 Imax : 0.7A (BMC)
 F_{sw} : 500KHz
 OCP : 3.5A ~5A
 soft star: 1.2ms

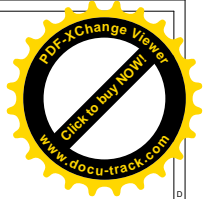
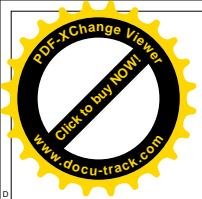


power rail: P1V0_STBY
 Vout: +1.0V
 Vin: +12V +5VSB_DUAL
 Imax : 0.7A (BMC)
 Ipeak: N/A
 F_{sw} : 500KHz
 OCP : 3.5A ~5A
 soft star: 1.2ms



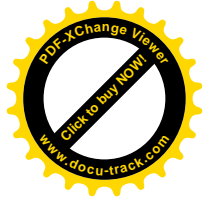
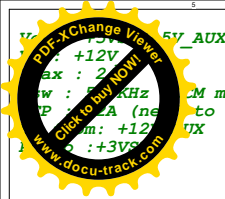
+3.3VSB -> +1.8V_AUX -> +3.3VSB_RGM
 +3.3VSB -> +1.8V_AUX -> +2.5V_AUX -> +1.2V_AUX -> +1.0V_AUX

Rev	BMC Power Rail
Created	2023/05/25
Drawn	Chen
Doc No.	Module_Schematic_21_000
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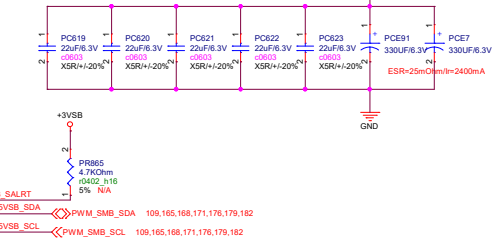
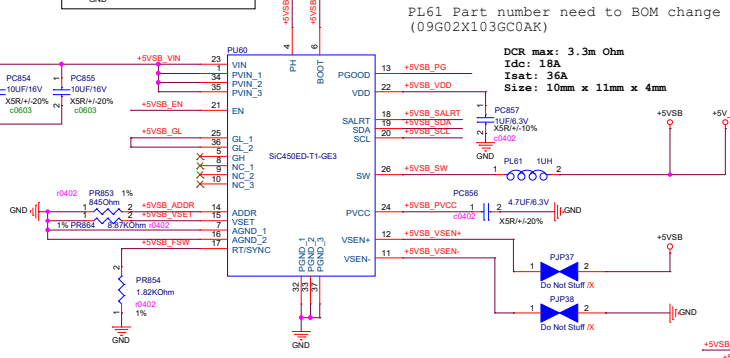
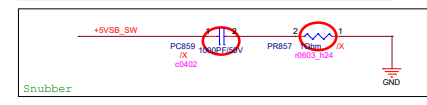
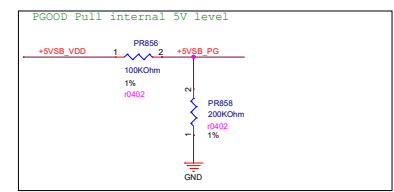
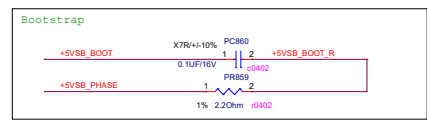
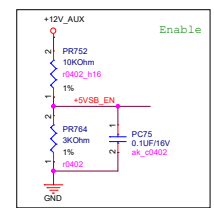
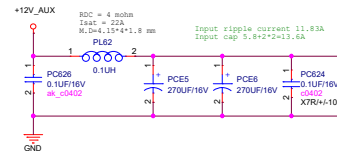


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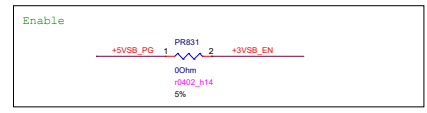
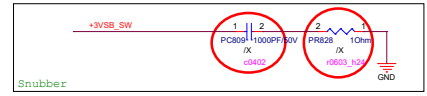
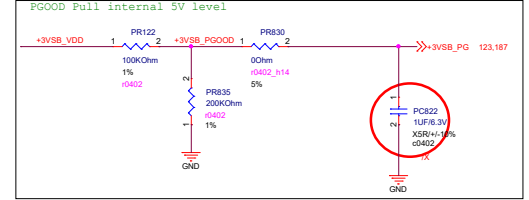
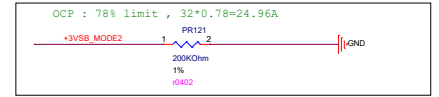
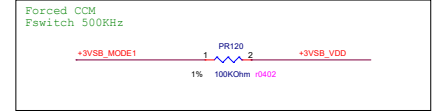
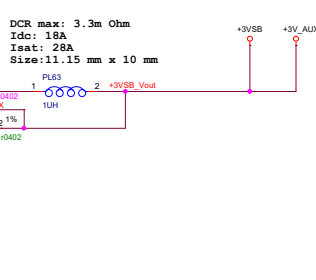
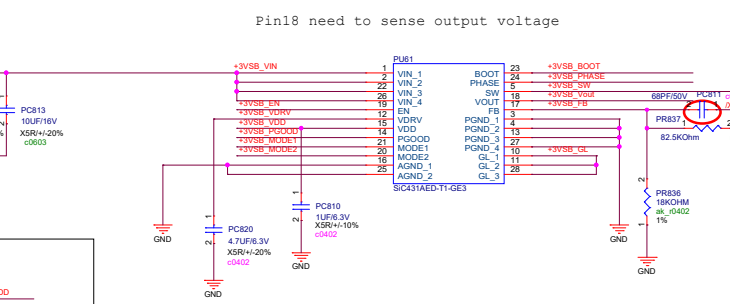
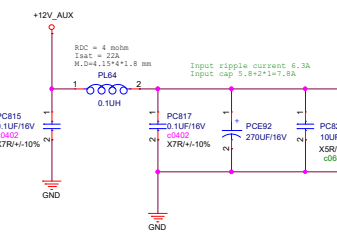
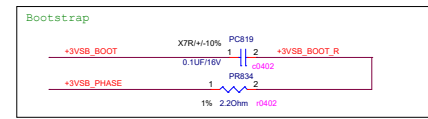
ASRock Rack		Title : <Title>	
<i>ASRock Rack</i>		Engineer: <i>Ryan Lu</i>	
Size	Project Name	Rev	
Custom	GENOA2D24TM3-2L+	R1.01	
Date: <i>Monday, November 21, 2022</i>		Sheet	188 of 213



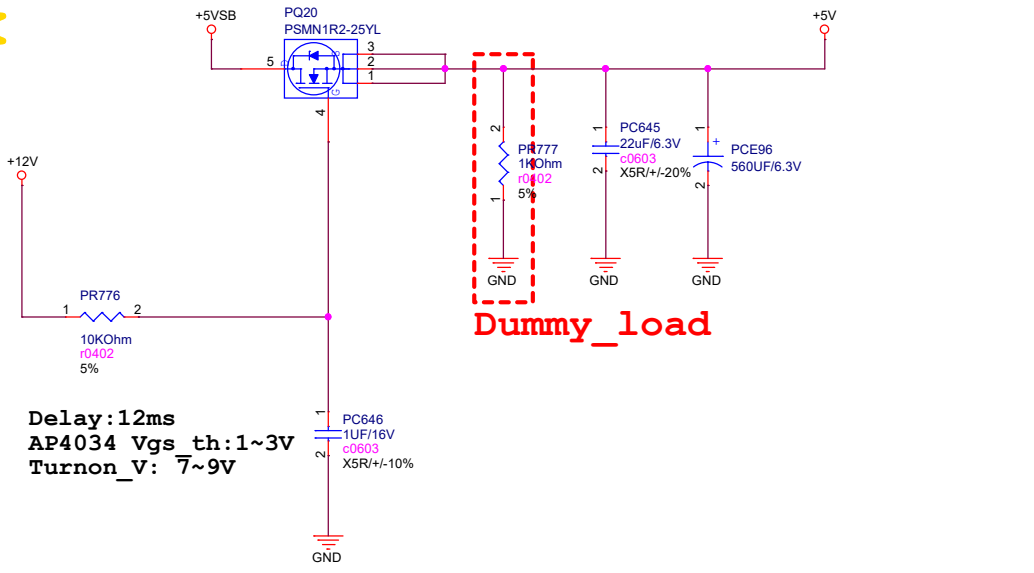
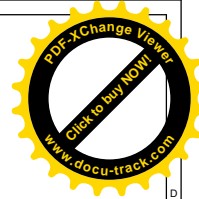
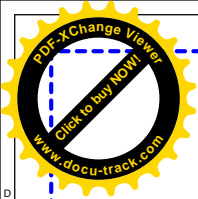
+12V AUX
 I_{max} : 2.14A
 F_{sw} : 500KHz
 Mode : FCCM mode
 OCP : 24.96A
 EN from : +12V AUX
 PG to : +3VSB



V_{out} : +3VSB/+3V_AUX
 V_{in} : +12V_AUX
 I_{max} : 14A
 F_{sw} : 500KHz FCCM mode
 OCP : 24.96A
 EN from : +5VSB_PG
 PG to : PWROK_P_S logic

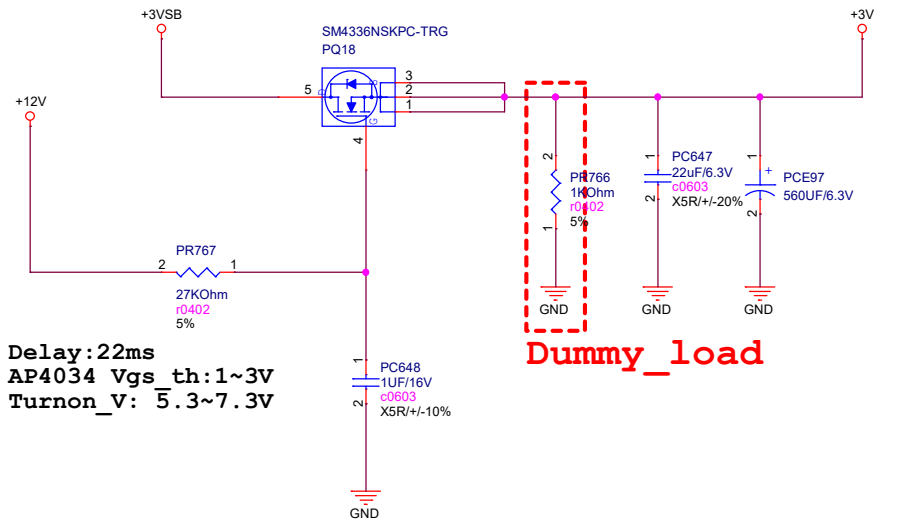


ASRock
Rock
 ASRock Rack
 Title : svsbVSB
 Engineer: Ryan Lu
 Project Name: GENOA2D24TM3-2L+
 Date: Monday, November 21, 2022
 Sheet: 189 of 213



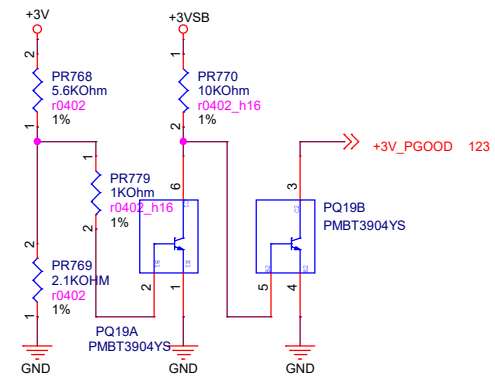
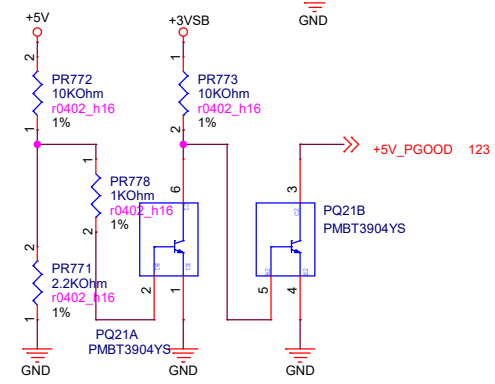
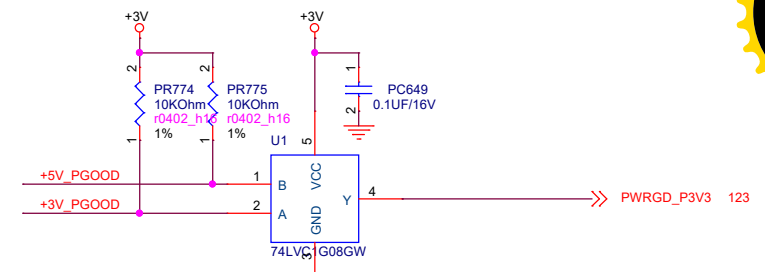
Dummy_load

+5V_Switch

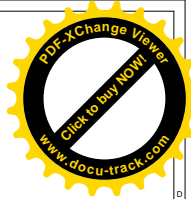
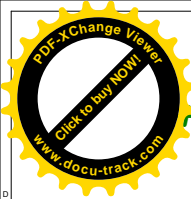


Dummy_load

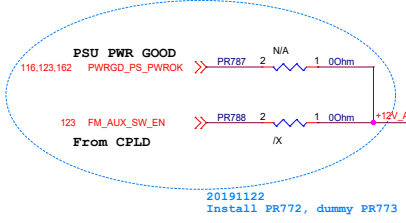
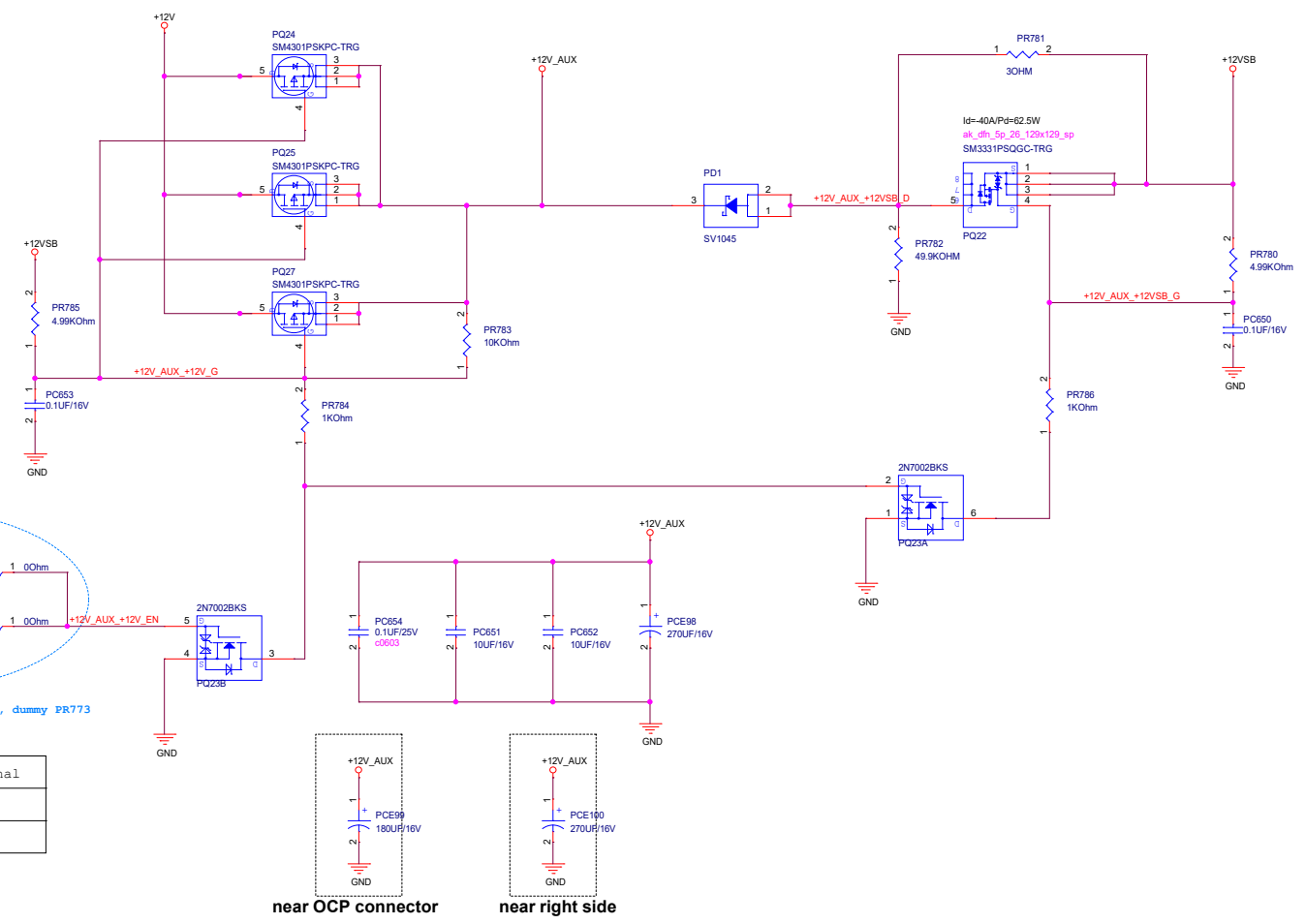
+3V_Switch



Title		+5V/+3V
Size	Document Number	Rev
B	<Doc>	R.1.0
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+12V_AUX



Vout	Signal
+12V	H
+12VSB	L

<Variant Name>

ASRock Rack Title : +12V_AUX
 ASRock Rack Engineer: Ryan Lu

Size	Project Name	Rev
Custom	GENOA2D24TM3-2L+	R1.01
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5

4

3

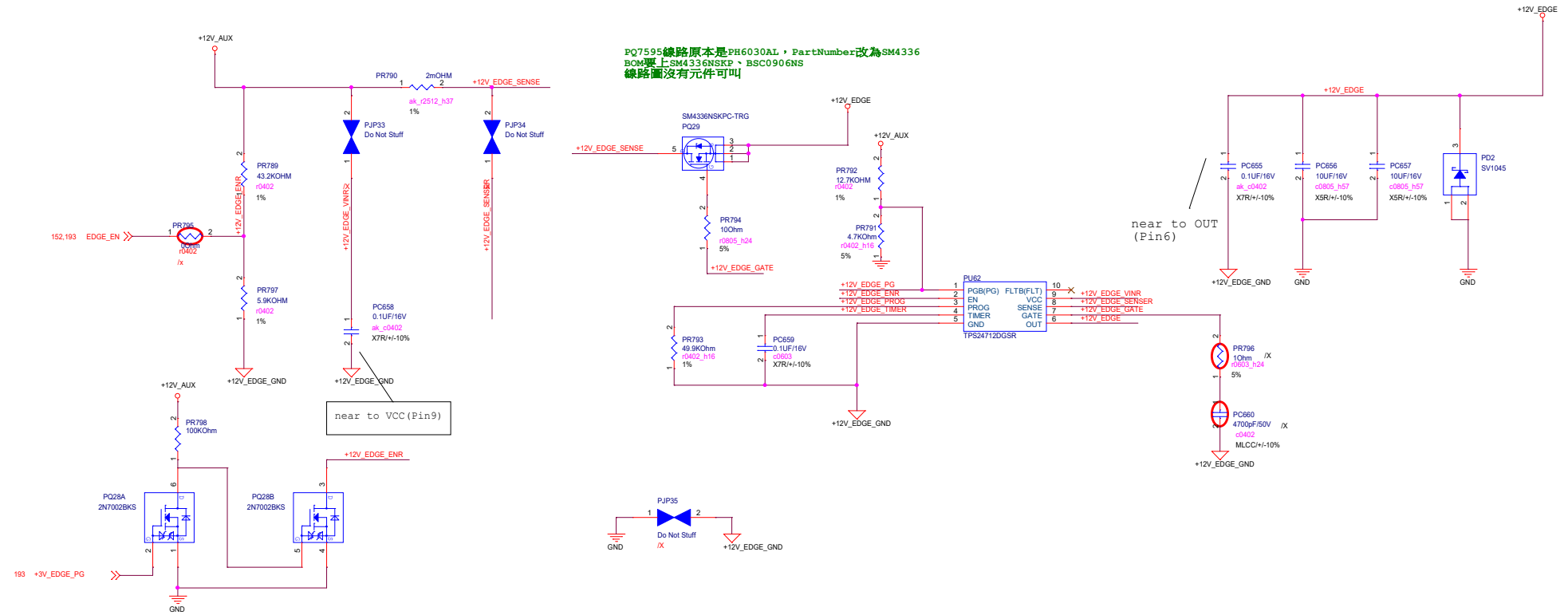
2

1



Power Rail : +12V_EDGE
 I_{OUT} : 1.5A
 I_{SENSE} : 13A

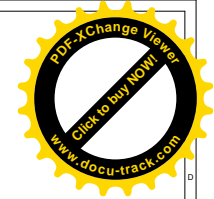
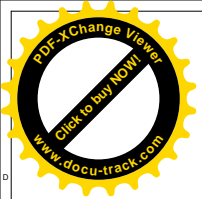
PQ7595 線路原本是 PH6030AL, PartNumber 改為 SM4336
 BOM 要上 SM433 GNSKB、BSC0906NS
 線路圖沒有元件可叫



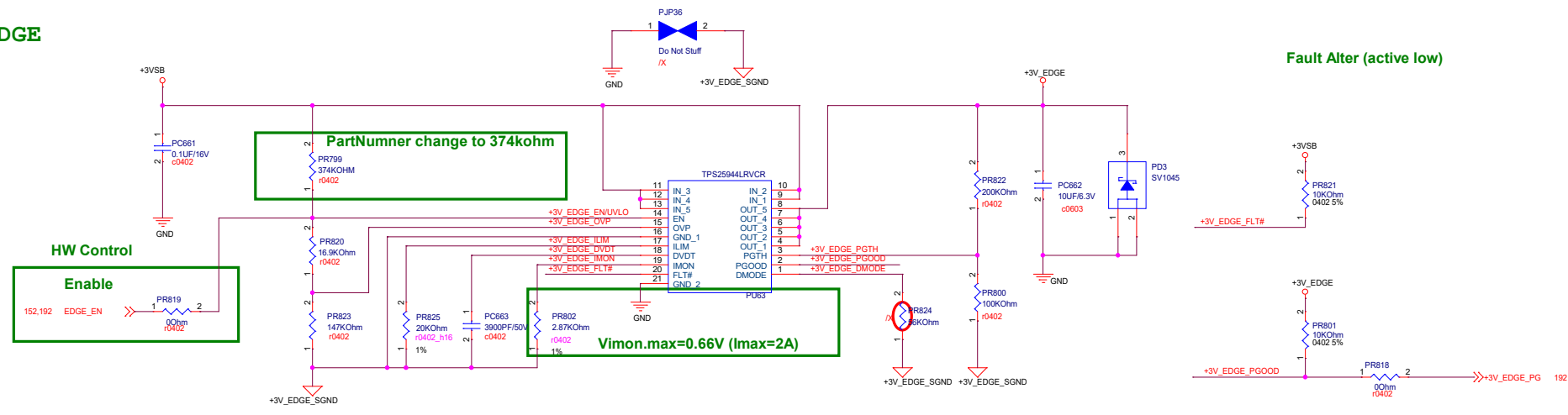
near to VCC (Pin9)

near to OUT (Pin6)

File	+12V_EDGE	
Size	Document Number	Rev
C	<Doc>	R1.0
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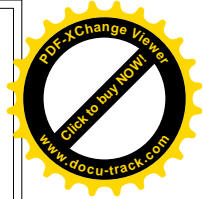
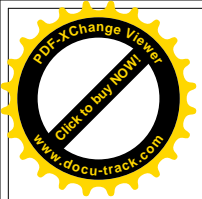


Power Rail :+3V_EDGE
 Io= 1.1A
 OCP :4.45A
 OVP: 3.6V
 UVP: 3V
 Cout=10uF
 Vpcth=3V




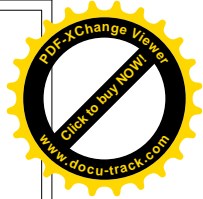
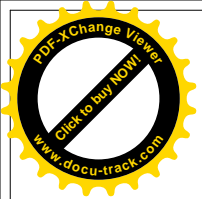
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ASRock Rack		Title : +3V_EDGE	
ASRock Rack		Engineer: Ryan Lu	
Size	Project Name	GENOA2D24TM3-2L+	
Custom		Date: Monday, November 21, 2022	Sheet 193 of 213
			Rev R1.01

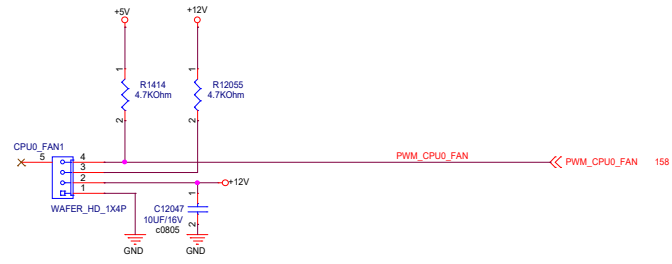


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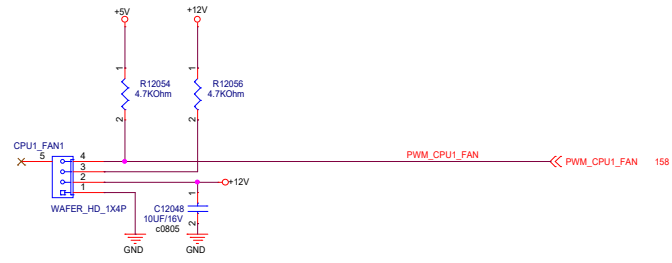
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ASRock Rack		Engineer: <i>Ryan Lu</i>	
Size	Project Name	Rev	
Custom	GENOA2D24TM3-2L+	R1.0	
Date: <i>Monday, November 21, 2022</i>		Sheet	184 of 218



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<Variant Name>

ASRock Rack		Title : CPU FAN CONN.	
ASRock Rack		Engineer: Ryan Lu	
Size C	Project Name GENOA2D24TM3-2L+	Rev R1.01	
Date: Monday, November 21, 2022		Sheet: 185	of 213