RAA229620

Digital Dual Output, 12-Phase Configurable, SVI3 PWM Controller

The RAA229620 is a digital dual output multiphase (X+Y ≤ 12) PWM controller designed to be compliant with AMD SVI3 specifications, targeting VDDCR_CPU and VDDCR_SOC rails. The high density dual output controller can be configured to support any desired phase assignment up to a maximum of twelve phases across the two outputs (X+Y). For example, 11+1, 10+2, 8+4, 6+6, or even single output operation as an 12+0 configuration are supported. The RAA229620 has a flexible X+Y ≤ 12 phase assignment and supports both the SVI3 interface and PMBus V1.3 interface, making it ideal for controlling the microprocessor core, graphics, and system rails for AMD SVI3 based platforms.

The RAA229620 uses the proprietary Renesas digital synthetic current modulation scheme to achieve the industry-best combination of transient response, ease of tuning, and efficiency across the full load range. Diode emulation and automatic phase add/drop features allow you to extract maximum efficiency from the converter regardless of load conditions. You can use the intuitive Renesas PowerNavigator™ software to configure and monitor the device.

With minimal external components, easy configuration, robust fault management, and highly accurate regulation capability, implementing a high-performance, multiphase regulator has never been easier.

Applications

- Core and system rails for AMD SVI3 systems
- High-performance graphics rails
- High-end desktops with over-clocking functions
- Networking, data center, and storage applications

Features

- Advanced linear digital modulation scheme
  - Auto phase add/drop with PFM mode for excellent load vs efficiency profile
  - Dual edge modulation with optional diode braking for faster transient response
  - Excellent VOTF performance
  - Zero latency synthetic current control for excellent high frequency current balance
- Supports the TLVR topology for capacitance reduction in high transient applications
- Differential remote voltage sensing supports ±0.5% closed-loop system accuracy over load, line, and temperature
- Highly accurate current sensing for excellent load-line regulation and accurate OCP
  - Supports the full range of Renesas Smart Power Stage (SPS) devices
- Comprehensive fault management enables high reliability systems
  - Pulse-by-pulse (per phase) and total output current limiting
  - Black Box status recording capability with first fault indicator
- Intuitive configuration using PowerNavigator
- SMBus/PMBus V1.3 compatible
- Up to 4 user configurations stored in device Non-Volatile Memory (NVM)

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1. Overview

1.1 Typical Application

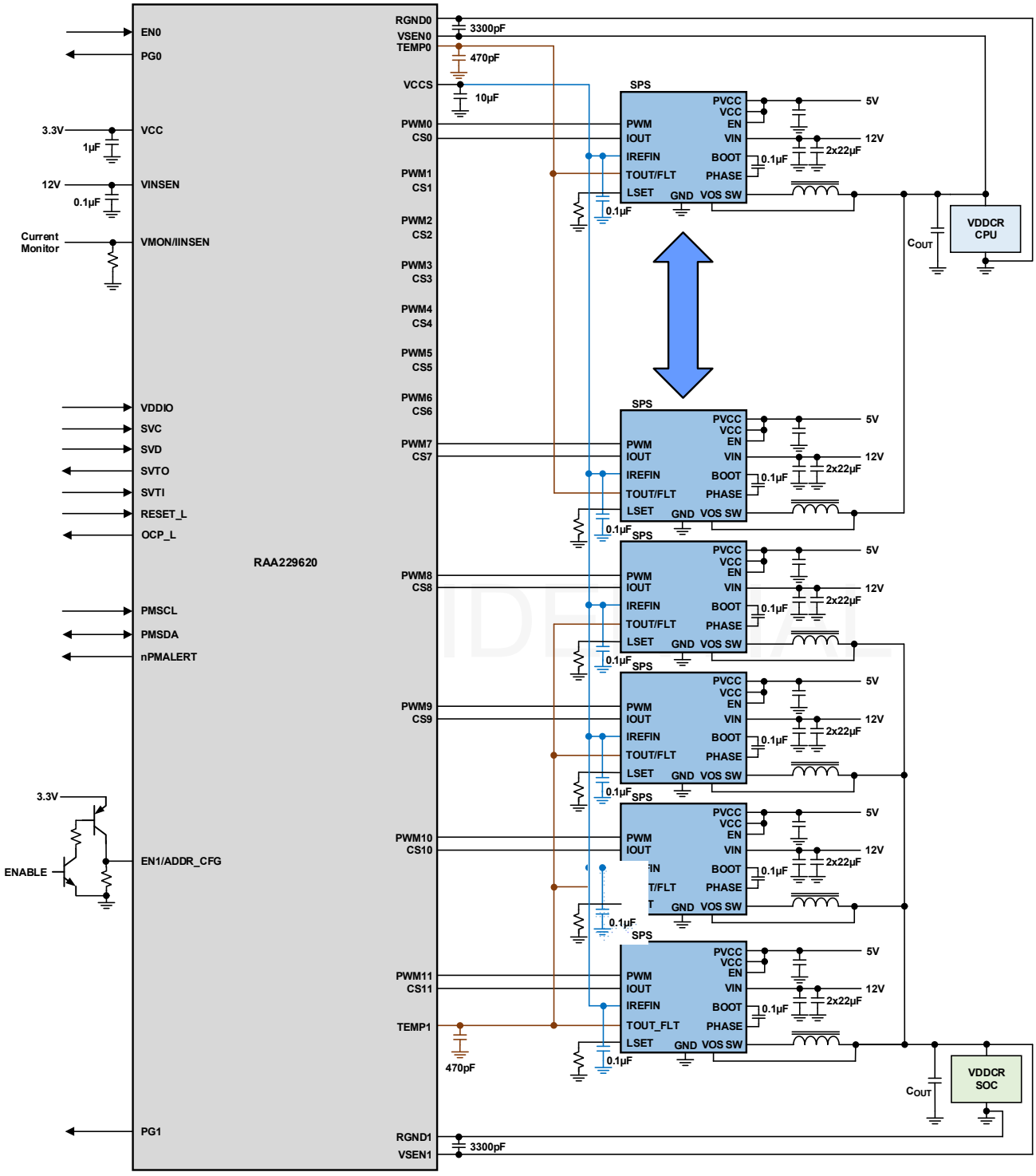


Figure 1. 8+4 Smart Power Stage

1.2 Block Diagram

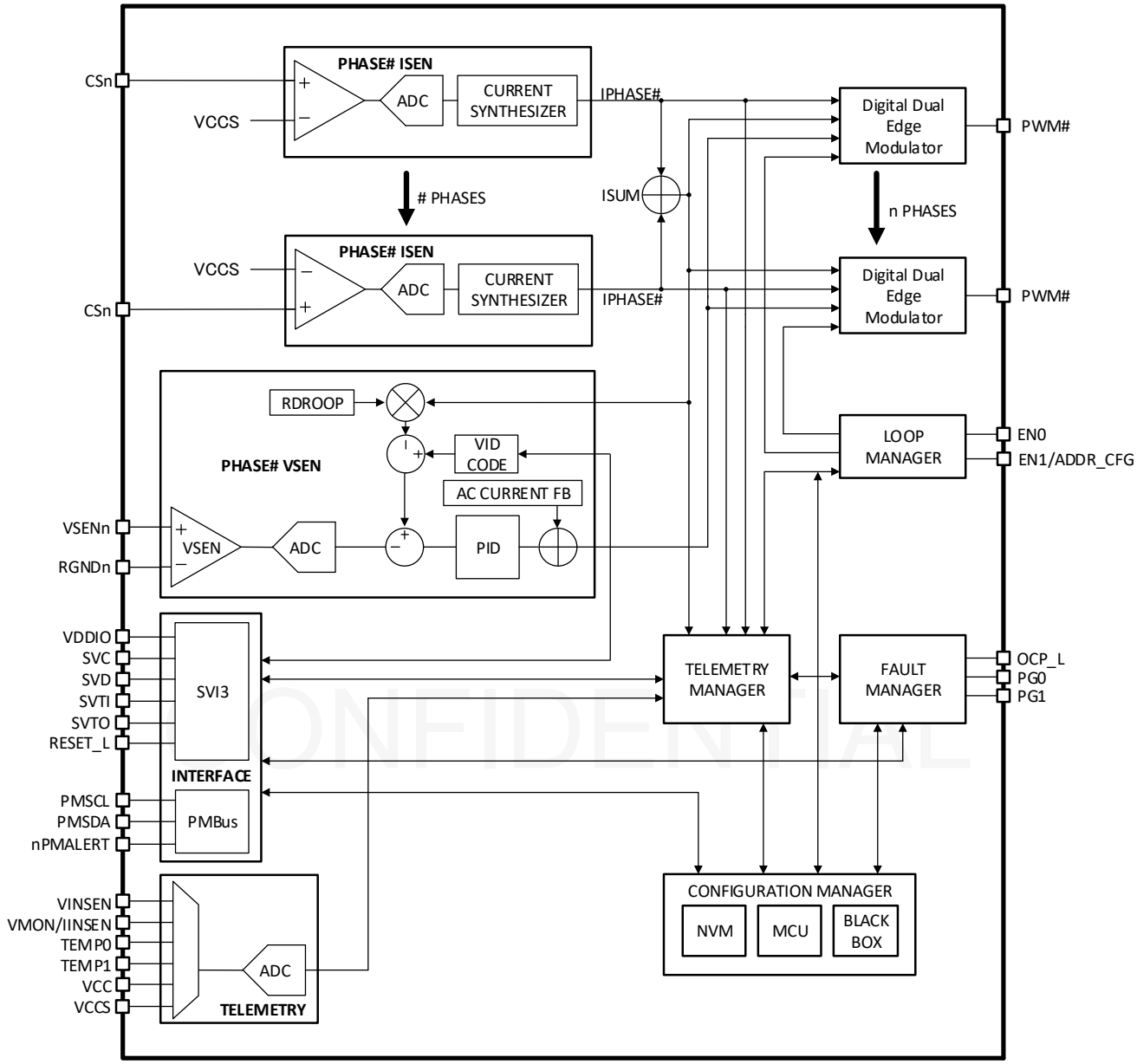
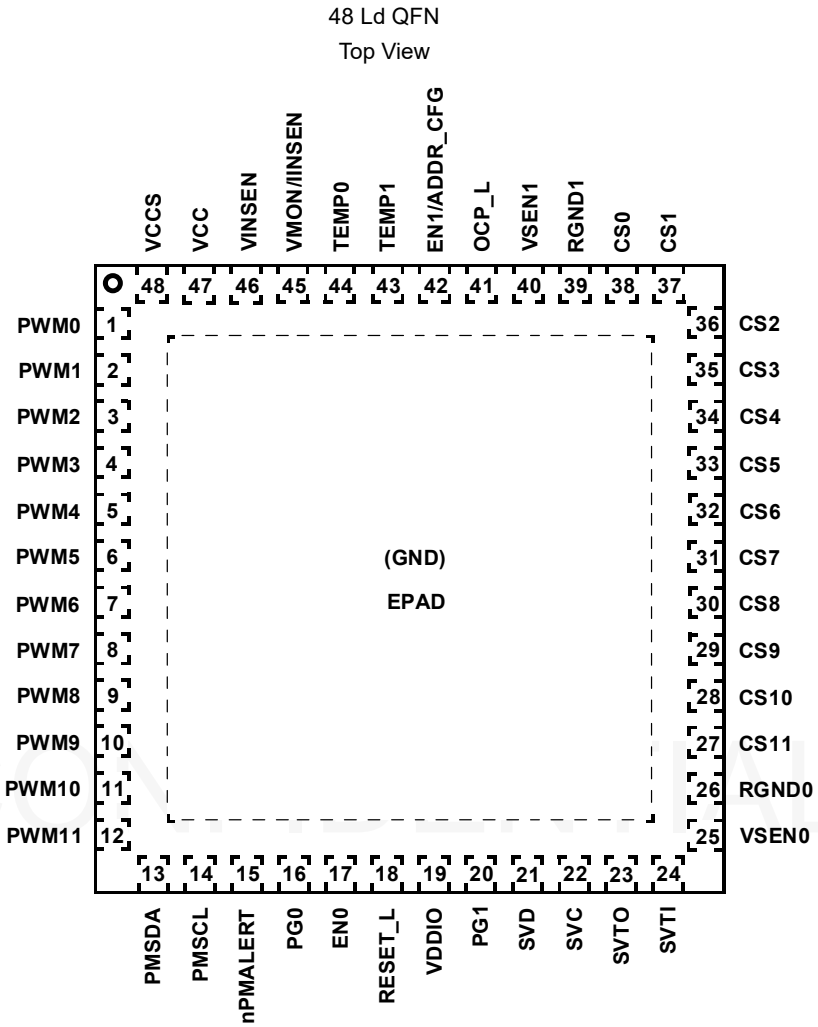


Figure 2. Internal Block Diagram

2. Pin Information

2.1 Pin Assignments



2.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	PWMx	Pulse-Width Modulation (PWM) outputs. Connect these pins to the PWM input pins of 3.3V logic-compatible smart power stages, driver ICs, or DrMOS. Leave floating if not used.
13	PMSDA	Serial data signal pin for the SMBus interface.
14	PMSCL	Serial clock signal pin for the SMBus interface.
15	nPMALERT	Open-drain output pin for alerting the SMBus host.
16, 20	PGx	Open-drain, power-good indicator for outputs.
17	EN0	Input pin that enables output 0.
18	RESET_L	Active low signal causing all SVI3 state machines and SVI3-defined registers to reset to default states.
19	VDDIO	SVI3 interface reference voltage input. Leave open if not used.
21	SVD	Serial VID Data is a push-pull signal which transmits commands from the master to the slaves.
22	SVC	Serial VID Clock is a push-pull signal which acts as a clock for SVD, SVTI and SVTO.
23	SVTO	Serial VID Telemetry Output is a push-pull output driven by each slave. It carries telemetry and acknowledge packets.
24	SVTI	Serial VID Telemetry Input is driven by the next-furthest slave (from the master) on the telemetry daisy-chain. It carries telemetry and acknowledge packets.
25, 40	VSENx	Positive differential voltage sense input for the outputs. Connect to the positive remote sensing point. Connect to ground if not used.
26, 39	RGNDx	Negative differential voltage sense input for the outputs. Connect to the negative remote sensing point. Connect to ground if not used.
27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38	CSx	Current-sense inputs to individual phase amplifiers. Unused phases should have their respective current-sense inputs grounded. Referenced to the VCCS supply. Supports smart power stage current sense.
41	OCP_L	Open-drain, active-low output that asserts when current is greater than SVI3 OCP_THRESH or OCP_WARN_THRESH
42	EN1/ ADDR_CFG	Input pin sets the SMBus/PMBus address and NVM configuration selection and to enable output 1. The pin senses a resistor to GND during configuration. When configuration is complete, the pin switches over to enable function. The pin must be transistor isolated from the enable circuit during resistor reading.
43, 44	TEMPx	Input pin for sensing external temperature measurement at outputs. Supports smart power stage sensing. Connect to ground if not used.
45	VMON/IINSEN	Multi-purpose pin. Input voltage sense pin for driver supply voltage when used as VMON. Current sense pin when used as IINSEN. The pin can connect to the positive side of a local input current sense resistor or it can sense the system input current from a ground referenced external current signal. Connect to ground if not used.
46	VINSEN	Input voltage sense pin for the V_{IN} supply voltage.
47	VCC	Chip primary bias input. Connect this pin directly to a +3.3V supply with a 1µF or greater MLCC bypass capacitor.
48	VCCS	Internally generated 1.2V LDO logic supply from VCC. Decouple with a 4.7µF or greater MLCC (X5R or better).
EPAD	GND	The package pad serves as the GND return for all device functions. Connect directly to the system GND plane with multiple vias.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Pins	Minimum	Maximum	Unit
Input Voltage Range	VCC		+4.3	V
	VCCS		+1.6	V
	VINSEN	GND - 0.3	18	V
	All Other Pins	GND - 0.3	V_{CC} + 0.3	V
ESD Rating	**Pins**	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	All Pins	2		kV
Charged Device Model (Tested per JS-002-2014)	All Pins	750		V
Latch-Up (Tested per JESD-78E; Class 2, Level A)	All Pins	100		mA

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
48 Ld 6x6 QFN Package	29	2.5

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{CC}	3.135	3.465	V
Junction Temperature	-40	+125	°C
Output Voltage	0	3.05	V

3.4 Electrical Specifications

Recommended operating conditions, V_{CC} = 3.3V, unless otherwise specified. **Boldface limits apply across the operating ambient temperature range -40°C to +85°C.**

Parameter	Test Conditions	Min[1]	Typ	Max[1]	Unit
V_{CC} Supply Current					
Nominal Supply Current	V_{CC} = 3.3V_{DC}; EN = V_{IH}, all Rails and phases operating, f_{SW} = 600kHz		60		mA
Shutdown Supply Current	V_{CC} = 3.3V_{DC}; EN = 0V, no switching		8		mA
VCCS LDO Supply					
Output Voltage			1.22		V
Maximum Current Capability	Excluding internal load		20		mA
Power-On Reset (POR)					
VCC Brownout Threshold			2.95		V
VCCS Rising POR Threshold			1		V
VCCS Falling POR Threshold			0.9		V
Enable Input High Level		**1.17**			V
Enable Input Low Level				**0.63**	V
Configurations Stored in Memory					
Number of Configuration Write Slots		**28**			
Number of Unique Configurations Stored		**4**			
POR to Initialization					
POR to Initialization Complete Time			10		ms
DAC (VID + Offset)					
System Accuracy[2]	Closed loop DAC = 1.00V to 3.05V, TJ = -40°C to 0°C	-0.5		0.5	%VID
	Closed loop DAC = 0.25V to 0.999V, TJ = -40°C to 0°C	-5		5	mV
	Closed loop DAC = 1.00V to 3.05V, TJ = 0°C to +85°C	-0.5		0.5	%VID
	Closed loop DAC = 0.25V to 0.999V, TJ = 0°C to +85°C	-5		5	mV
	Closed loop DAC = 1.00V to 3.05V, TJ = 85°C to +125°C	-0.5		0.5	%VID
	Closed loop DAC = 0.25V to 0.999V, TJ = 85°C to +125°C	-5		5	mV
Voltage Sense Amplifier					
Open Sense Current	Only at VSEN open detection during initialization period		220		µA
Input Impedance (VSEN-RGND)			140		kΩ

Recommended operating conditions, V_{CC} = 3.3V, unless otherwise specified. **Boldface limits apply across the operating ambient temperature range -40°C to +85°C. (Cont.)**

Parameter	Test Conditions	Min[1]	Typ	Max[1]	Unit
Maximum Common-Mode Input			V_{CC} - 0.2		V
Differential Input Range (VSEN-RGND)				**3.05**	V
Output Current-Sense and Overcurrent Protection					
Current Sense Accuracy	SPS configuration	**-1**		**1**	%
Average Overcurrent Threshold Resolution			0.1		A
Cycle-by-Cycle Current Limiting Threshold Resolution			0.4		A
Digital Droop					
Droop Resolution			0.01		mV/A
Oscillators					
Accuracy of Switching Frequency Setting			±2		%
Switching Frequency Range		**0.2**		**2.0**	MHz
Soft-Start Rate and VOTF Rate					
Minimum Soft-Start Ramp Rate	Programmable minimum rate		0.01		mV/µs
Maximum Soft-Start Ramp Rate	Programmable maximum rate		100		mV/µs
Soft-Start Ramp Rate Accuracy			±2		%
Minimum Dynamic Slew Rate			0.01		mV/µs
Maximum Fast Dynamic Slew Rate			100		mV/µs
Dynamic Slew Rate Accuracy		**-4**		**4**	%
PWM Outputs					
PWMx Output High Level	I_{OUT} = 4mA	**V_{CC} - 0.4**			V
PWMx Output Low Level	I_{OUT} = 4mA			**0.4**	V
PWMx Tri-State Leakage (pin forced high)	V_{PWM} = V_{CC}			**1**	µA
PWMx Tri-State Leakage (pin forced low)	V_{PWM} = 0V	**-1**			µA
Thermal Monitoring and Protection					
Temperature Sensor Range		**-50**		**150**	°C
Temperature Sensor Accuracy	SPS configuration		±4.5		%
Power-Good and Protection Monitors					
PG Output, OCP_L Low Voltage	I_{OUT} = 4mA load			**0.2**	V
PG, OCP_L Leakage Current	With a pull-up resistor externally connected to VCC		5		µA
Overvoltage Protection Threshold Resolution			1		mV

Recommended operating conditions, V_{CC} = 3.3V, unless otherwise specified. **Boldface limits apply across the operating ambient temperature range -40°C to +85°C. (Cont.)**

Parameter	Test Conditions	Min[1]	Typ	Max[1]	Unit
Undervoltage Protection Threshold Resolution			1		mV
Input Current-Sense and Catastrophic Failure Protection (CFP) Output					
Input Voltage Accuracy	VINSEN to ADC accuracy		±2.5		%
Input Overvoltage Threshold Resolution			16		mV
SVI3 Bus					
VDDIO Voltage Range		1.08		1.98	V
SVC, SVD, SVTI Input High Level		**0.65 * V_{DDIO}**			V
SVC, SVD, SVTI Input Low Level				**0.35 * V_{DDIO}**	V
SVC, SVD, SVTO Output High Level	I_{OUT} = 4mA	**V_{DDIO} - 0.22**			V
SVC, SVD, SVTO Output Low Level	I_{OUT} = 4mA			**0.22**	V
SVC Frequency Range		**5**		**50**	MHz
RESET_L Input High Level		**1.17**			V
RESET_L Input Low Level				**0.63**	V
SMBus/PMBus					
nPMALERT, PMSDA Output Low Level	I_{OUT} = 20mA			**0.4**	V
PMSCL, PMSDA Input High Level		**1.35**			V
PMSCL, PMSDA Input Low Level				**0.8**	V
PMSCL, PMSDA Input Hysteresis			80		mV
PMSCL Frequency Range		**0.01**		**2.00**	MHz

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. These parts are designed and adjusted for accuracy with all errors in the voltage loop included. Verified by design and/or characterization.

4. Initializing the Device

4.1 Power-On Reset (POR)

RAA229620 initialization begins after V_{CC} crosses its rising POR threshold. When POR conditions are met, basic digital subsystem integrity checks begin. During this process, the controller starts the telemetry subsystem, configures its PMBus address and loads the selected user configuration from NVM according to the EN1/ADDR_CFG pin resistor value, checks fault status, and prepares for regulation. When the device is configured, the EN1/ADDR_CFG pin is reconfigured to operate as an enable pin for output 1. The PWM pins are held in tri-state until the device is commanded to regulate. Figure 3 shows the device initialization sequence.

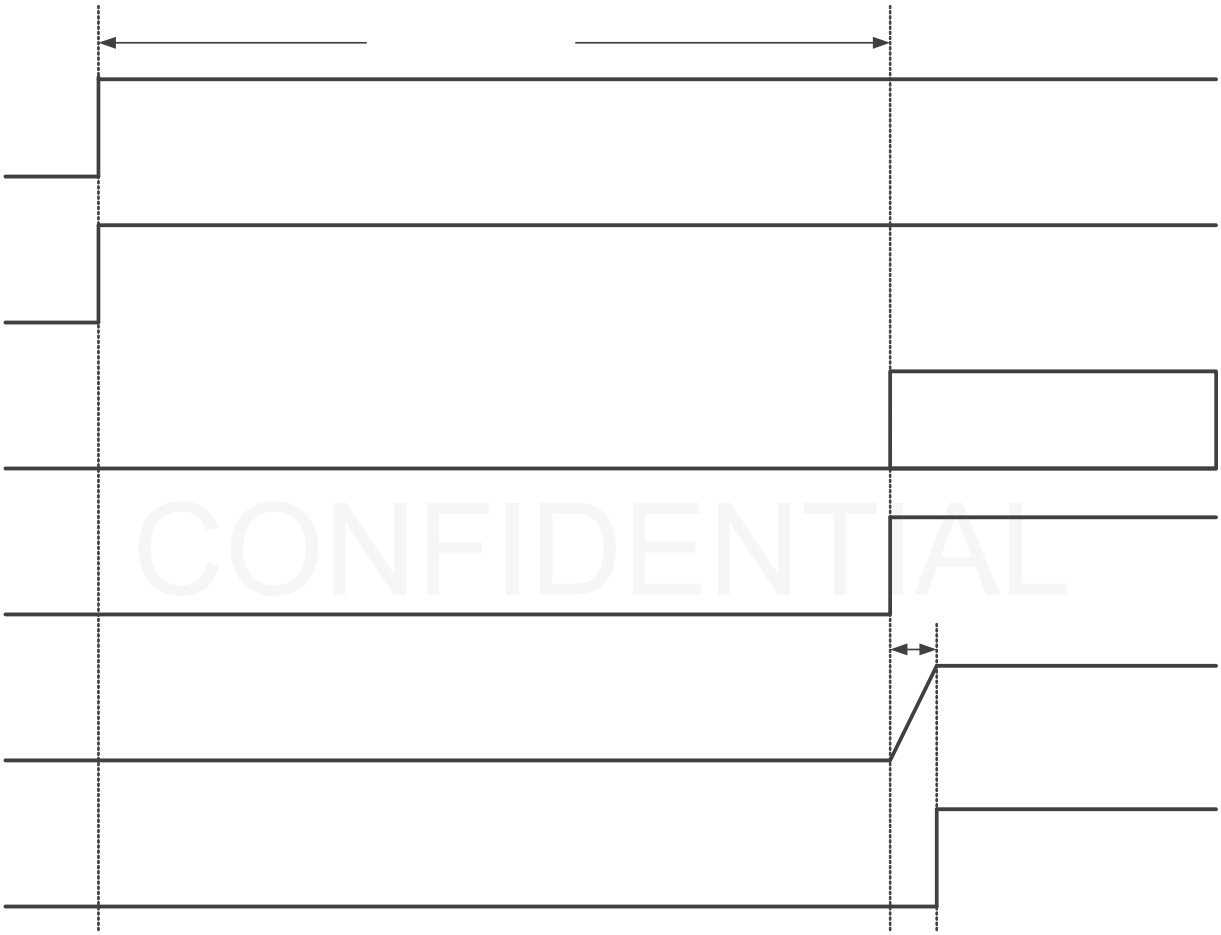


Figure 3. Simplified PMBus Initialization Timing Diagram

4.2 Selecting the PMBus Address and User Configuration

The EN1/ADDR_CFG pin reads the value of a resistor connected to GND to determine the NVM configuration to load and the PMBus address to use during host communication. Table 1 shows the R_{ADDR_CFG} values to specify the configuration ID and the PMBus slave address (7-bit).

Table 1. Resistor Value to PMBus Address and User Configuration ID Map

R Value (Ω)	PMBus Address	Configuration ID
681	61	0
887	61	1
1130	61	2
1370	61	3
1650	62	0
1960	62	1
2320	62	2
2670	62	3
3090	63	0
3570	63	1
4120	63	2
4640	63	3
5230	72	0
5900	72	1
6650	72	2
7500	72	3
8450	74	0
9530	74	1
10700	74	2
12100	74	3
13700	75	0
15400	75	1
17400	75	2
19600	75	3
22100	76	0
24300	76	1
27400	76	2
30100	76	3

4.3 NVM User Configurations

The RAA229620 supports four distinct configuration identifiers selected by the EN1/ADDR_CFG pin. Table 1 provides the R_{ADDR_CFG} value corresponding to each configuration identifier. A total of 28 one-time programmable non-volatile memory locations are available to store new user configurations or overwrite existing ones. With this flexibility, all four unique configurations can be written up to seven times, one configuration ID can be written up to 28 times, or any combination of configuration IDs can be written until the 28 write limit is reached. Only the most recent configuration for a given configuration ID can be loaded. When all 28 memory locations have been written, the RAA229620 no longer accepts attempts to write to NVM. PowerNavigator provides a simple interface to store and load configurations.

4.4 Configuring the Device

RAA229620 configuration is accomplished by generating a configuration file using PowerNavigator and either directly loading to the device RAM or programming to the device NVM. During device initialization, the IC attempts to load a configuration from NVM. If no configuration is found, the device remains in a wait state with the PWM pins tri-stated. The device ignores attempts to enable and waits until a configuration is directly loaded using PowerNavigator. The IC features and functions described in this datasheet are all configured using PowerNavigator. The datasheet provides fundamental understanding of device behavior and design information. Additional details regarding the configuration process is provided in PowerNavigator.

5. Operating the Device

After the RAA229620 initializes and a configuration is loaded, it is ready for operation.

The RAA229620 has several performance enhancing features that enable it to meet the most stringent voltage regulation and efficiency demands. The synthetic current modulator provides excellent transient response to support the latest generation of ASICs and CPUs. Automatic phase dropping, diode emulation, and PFM operation improve efficiency across the load range. The RAA229620 supports Smart Power Stage (SPS) current sense to enable optimal design. The device also supports a full complement of high resolution telemetry. The following sections provide more detail about these features.

5.1 Input Voltage Sensing

Input voltage is monitored using the VINSEN pin that should be connected as shown in Figure 4.

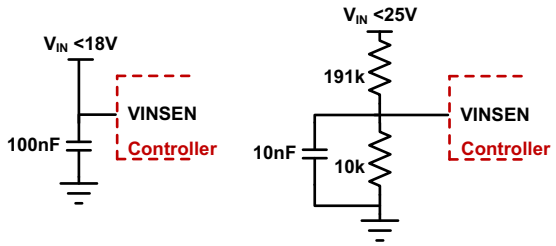


Figure 4. Input Voltage Sense Configuration

Input voltage is monitored continuously, and regulation is stopped anytime the sensed input voltage falls outside the boundaries established by configuration settings associated with the parameters V_{IN} ON, V_{IN} OFF, V_{IN} overvoltage fault limit, and V_{IN} undervoltage fault limit.

5.2 Lossless Input Current and Power Sensing

Input current telemetry is provided per rail using an input current synthesizer. By using the ability of the RAA229620 to precisely determine its operational conditions, input current can be synthesized to a high degree of accuracy without the need for a lossy sense resistor. With a precise knowledge of input current and voltage, input power can be computed.

5.3 VMON Voltage Sensing

The VMON/IINSEN input pin, when configured for VMON, provides a secondary input voltage sense with several selectable voltage ranges. The VMON input pin can inhibit rail operation when the sensed voltage falls outside the boundary established by the configuration settings that are associated with the parameters VMON_ON and VMON_OFF. If a rail is prevented from operating because of a VMON excursion, the rail restarts if the sensed voltage returns to the specified range. Use of this feature is optional for each rail. A typical use case for this voltage sensing feature is monitoring the bias supply voltage associated with the power stages and preventing operation if this voltage is below the configured range. Connection of the VMON pin for sensing the 5V SPS bias voltage is shown in Figure 5.

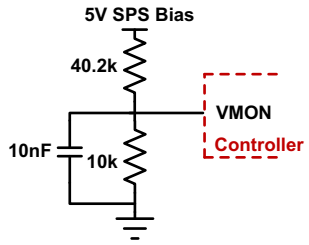


Figure 5. VMON Configuration

5.4 Input Current Sensing for NVDIMM

When configured for IINSEN, the VMON/IINSEN input pin is combined with the VINSEN pin to form a differential input that is used with a shunt resistor to support NVDIMM applications. See Figure 6 for connection details.

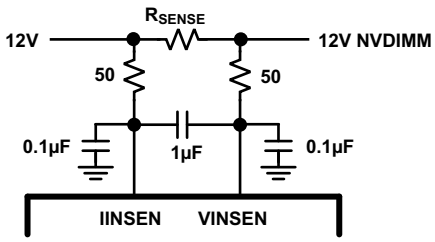


Figure 6. NVDIMM Configuration

5.5 Enabling and Soft-Starting the Device

The RAA229620 outputs are enabled using the enable pin or PMBus. Enable method selection is configured in PowerNavigator on a per rail basis. When the RAA229620 is commanded to regulate an output, it begins its soft-start sequence. Soft-start moves V_{OUT} smoothly to the programmed default voltage. Soft-start timing is programmed using the TON_DELAY (60h) and TON_RISE (61h) PMBus commands while in PMBus mode. While configured as an SVI3 rail, soft-start timing is controlled by the SVI3 interface.

If a pre-existing voltage bias exists on the output, the PWM signals are held in tri-state until the soft-start ramp reaches the prebias level. The tri-state prevents the converter from sinking current and pulling the prebias down. No special configuration is required to enable this operation.

5.6 Disabling the Device

Similar to the enabling process, outputs can be disabled using the enable pin or PMBus on a per rail basis. The RAA229620 can be configured to disable in two ways:

- Immediate OFF: Immediately ceases regulation and tri-states PWM pins
- Soft OFF: Actively ramps the output voltage down to 0V before ceasing activity as programmed in TOFF_DELAY (64h) and TOFF_FALL (65h) PMBus commands while in PMBus mode. While configured as an SVI3 rail, soft-start timing is controlled by the SVI3 interface.

5.7 Phase Configuration and Automatic Phase Dropping

The RAA229620 supports two regulated outputs that control its 12 phases. Each rail is capable of controlling up to 12 phases, but the rails can be configured for fewer phases. Unused phases should have their CS pins grounded.

The RAA229620 supports Automatic Phase Dropping (APD) to optimize efficiency across the load range. Figure 7 shows the typical characteristics of efficiency vs load current as the phase count is varied. The diagram shows that optimal efficiency is achieved by using fewer phases as the load current decreases.

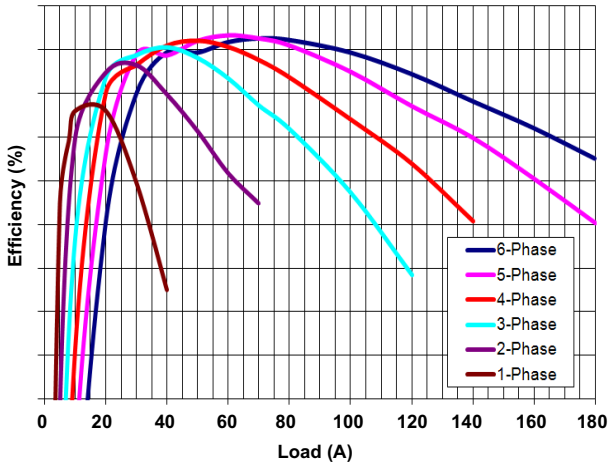


Figure 7. Efficiency vs Phase Number

The RAA229620 continuously monitors output current, and if APD is enabled, the device drops or adds phases from use as the load current varies.

Phases are dropped one at a time with a user programmed delay between drop events. For example, if the delay is set to 1ms, eight phases are active, and the load suddenly drops to a level needing only one phase; the RAA229620 begins by dropping a single phase after 1ms. An additional phase is dropped each millisecond until only one phase remains active. On Rail 0, phases are dropped beginning with the highest assigned phase. On Rail 1, phases are dropped beginning with the lowest assigned phase.

Phases are automatically returned to service when load conditions require more phases. The phases are returned to service in the opposite order they were dropped. Conditions that result in phase adding include increased load current, rapid change sensed on the output voltage, and VOTF events. When rapid change is sensed on the output voltage, the Fast Phase Add function prepares all dropped phases for activation so there is no delay if all phases are needed to support a load transient.

Any command to change the output voltage set point uses all phases, including VOTF events. After the output voltage change is complete, phases begin dropping as configured.

To ensure dropped phases have sufficient bootstrap capacitor charge to turn on the high-side MOSFET after a long period of inactivity, a bootstrap refresh function periodically turns on the low-side MOSFET of each dropped phase to refresh the bootstrap capacitor.

5.8 SVI3 Power State and Automatic Phase Dropping

To produce the most optimal efficiency across a wide range of output loading, the modulator supports automatic dropping or adding of phases and diode emulation (in a single-phase state). Use of APD and diode emulation are optional. If automatic phase dropping is enabled, the number of active phases at any time is determined solely by load current. In this case, the specific power state indicated through SVI3 has no effect on phase count. If APD is disabled, the power state commanded through SVI3 determines the number of active phases. Regardless of APD enable state, the controller always adds phases to support the load current demand, protecting the application if APD is disabled in a low phase count state.

The RAA229620 supports six distinct power states as shown in Table 2. The regulator starts up into PS0 and lower power states can only be entered after successful start-up.

Table 2. Power State Command from CPU

Power State	Behavior with APD Disabled	Behavior with APD Enabled
PSI0	Use all configured phases as minimum phase count (default)	Drop phases to minimum required by load current using programmed minimum phase count.
PSI1	Use the phase count dictated by SVI3 register PHASE_SHED_1 and add phases if load current requires it. If phases need to be added, they remain added.	Drop phases to minimum required by load current using programmed minimum phase count.
PSI2	Use the phase count dictated by SVI3 register PHASE_SHED_2 and add phases if load current requires it. If phases need to be added, they remain added.	Drop phases to minimum required by load current using programmed minimum phase count. If minimum phase count = 1, diode emulation and PFM are also used.
PSI3	Single phase operation + diode emulation and PFM	Drop phases to minimum required by load current using programmed minimum phase count. If minimum phase count = 1, diode emulation and PFM are also used.
PSI4	Single phase operation + diode emulation and PFM	Drop phases to minimum required by load current using programmed minimum phase count. If minimum phase count = 1, diode emulation and PFM are also used.
PSI5	Not Supported - NACK and set error bits in SVI3 NACK_STATUS	Not Supported - NACK and set error bits in SVI3 NACK_STATUS
PSI6	Ramp or decay down to 0V (voltage regulation disabled). PWRGD pin remains asserted. All nonessential systems are shutdown.	Ramp or decay down to 0V (voltage regulation disabled). PWRGD pin remains asserted. All nonessential systems are shutdown.
PSI7	Drop phases to minimum required by load current using programmed minimum phase count. If minimum phase count = 1, diode emulation and PFM are also used.	Drop phases to minimum required by load current using programmed minimum phase count. If minimum phase count = 1, diode emulation and PFM are also used.

5.9 Diode Emulation and PFM Operation

As described in SVI3 Power State and Automatic Phase Dropping, the RAA229620 supports APD to optimize phase usage as load demand decreases. When the regulator drops to 1-phase operation, it supports diode emulation and PFM (Pulse Frequency Modulation) operation to further maximize efficiency performance. Traditionally, use of such efficiency boosting techniques have come at the expense of transient response, but the RAA229620 is able to meet all transient demands directly from diode emulation/PFM operations. The RAA229620 offers optimal efficiency performance independent of the host commanded power state.

Diode emulation and PFM operation are supported when a single phase is active. If constant frequency operation is needed at light loads, the feature can be disabled. If enabled, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow a reverse current, emulating an ideal diode. As Figure 8 shows, when the inductor current is positive, the LGATE is held on, allowing current to flow in the low resistance channel

of the LFET. When current reaches 0, the LFET is turned off to prevent a reverse current in the inductor. The controller modulates the LFET state through the PWM pin of the respective regulator channel by tri-stating the PWM when the load current reaches zero, which commands the MOSFET driver to turn off both the HFET and LFET.

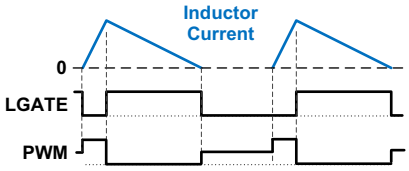


Figure 8. Diode Emulation PWM Signaling

In single-phase diode emulation operation, the RAA229620 delivers inductor current pulses with a user programmed pulse width. By programming the pulse width, the output voltage ripple can be tuned to meet expectations for any system type. Pulse frequency is then modulated to maintain output voltage regulation, which is depicted in Figure 9. The transition from single phase PFM to multiphase constant frequency operation is managed seamlessly by the IC.

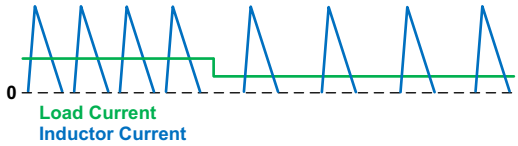


Figure 9. Single Phase Light Load PFM Operation

5.10 Diode Braking

Applications that support loads with large transient current demands often have significant output voltage overshoot when the load current demand drops suddenly. In some cases, diode-braking may allow overshoot reduction at the expense of thermal dissipation in the low-side MOSFET.

5.11 Load-Line Saturation

A load line achieves a better load transient response with less output capacitance because of a bigger output voltage window. In a typical load line system, as soon as the load current changes from 0A, the controller applies the load-line function to the output voltage. The output voltage at the minimum operating current of the ASIC lies within a V_{MAX} to V_{MIN} window. However at no-load, with a traditional load line, the output voltage can exceed the V_{MAX} rating of the ASIC. To prevent this, the RAA229620 provides the load-line saturation feature.

With the load-line saturation feature, a user can program a current below so that the load-line function is no longer applied to the output voltage, which saturates the load line. For example, if the slope of the load line is set to 0.1mΩ and the typical leakage current of the ASIC is 200A, V_{MAX} = 0.815V and V_{MIN} = 0.75V. Applying load line over the entire load current range could cause the output voltage to increase beyond the V_{MAX} limit at no-load. Setting the load-line saturation current to 200A does not apply the load-line function to the output voltage if the load reduces below 200A as shown in Figure 10.

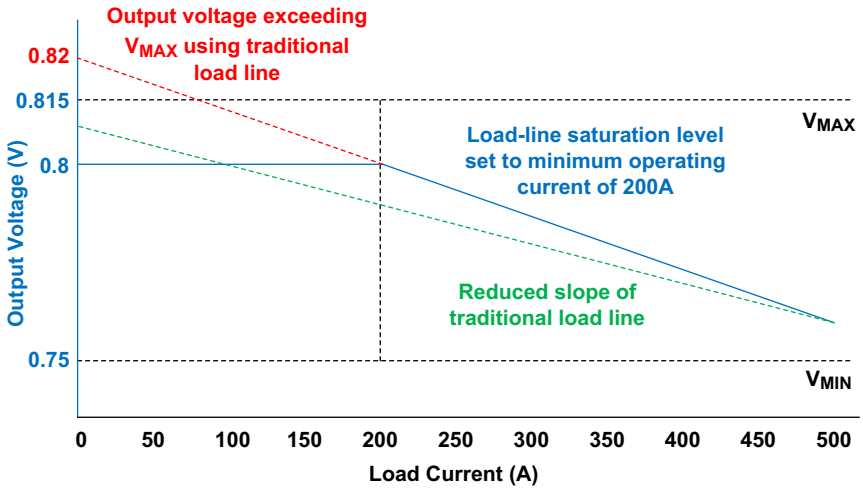


Figure 10. Load-Line Saturation

Another advantage of the load-line saturation feature is the provision of a steeper load line that further reduces the amount of output capacitance required. In a traditional load line, no-load output voltage can be prevented from exceeding V_{MAX} by reducing the slope of the load line as shown in Figure 10. This reduction of slope also reduces the output voltage window for a load transient, so it requires more output capacitance as compared to a load-line saturation.

5.12 Switching Frequency

Switching frequency is independently programmable on each rail from 200kHz to 2MHz.

5.13 Output Current Sensing

The RAA229620 supports Smart Power Stage (SPS) current sensing. Connection to the SPS is accomplished through the CS pins, the SPS IMON output is connected to the corresponding RAA229620 CSn input. CS pins are referenced to the VCCS supply which must be connected to the SPS current sense reference voltage. For connection details, see the typical application diagram shown in Figure 1.

5.14 Temperature Sensing

The RAA229620 monitors internal die temperature and supports external SPS temperature sense. The RAA229620 can be configured to sense SPS temperature on a per-rail basis by tying together the TMON/FLT pins of all the SPS on a configured rail and connecting them to the TEMPx pins.

6. Fault Monitoring and Protection

The RAA229620 includes an extensive fault management system that integrates with high performance host controllers, supporting unprecedented remote system management and debugging capability. In the event of a fault condition, the IC deasserts the PG pin associated with the faulted rail and alerts the host using the PMAlert pin. The RAA229620 also provides a black box recorder with extensive fault logging to support system level debug.

Fault controls are independently enabled and associated fault responses are user configurable. Response type is independently configurable by fault type. Response types supported are:

- **Alert only**: The rail continues to operate.
- **Shut down immediately**: The rail is latched off until commanded on.
- **Shut down and retry with variable retry delay**: The rail attempts to retry indefinitely until the condition clears or the rail is commanded off.

When a fault condition has been declared, clear the fault by issuing a CLEAR_FAULTS command or by cycling the EN pin of the faulted rail.

6.1 Power-Good Signals

The PG pins are open-drain, power-good outputs that indicate completion of the soft-start sequence and output voltage of the associated rail within the expected regulation range. In the event of a fault, the PG pin of the associated rail is pulled low. PG is also pulled low immediately upon a rail disable.

6.2 Overvoltage/Undervoltage Protection

Output voltage is measured at the load sensing points differentially for regulation, and the same measurement is used for OVP and UVP. The output voltage comparisons are done in the digital domain. Figure 11 depicts the overvoltage and undervoltage thresholds as they relate to the enabling of the IC and to dynamic output voltage changes.

The RAA229620 can be configured to have active OVP with a user configurable threshold in the disabled state. The UV threshold is always VID tracking and is active only while the rail is regulating. When enabled, OV threshold transitions to VID tracking.

An undervoltage fault is declared if V_{OUT} falls below the configured UV threshold.

If V_{OUT} exceeds the OV threshold and is configured to have a protection response, the IC employs a soft crowbar technique to manage V_{OUT}. This method of OV protection pulses the LFET until the output voltage is pulled down to 100mV below the VID tracking limit. For instance, if a device is configured with a 400mV threshold above VID, the LFET would be held on until V_{OUT} is 100mV below the threshold. Figure 11 depicts this voltage window as “soft crowbar hysteresis”. If V_{OUT} rises again after the LFET is turned off and hits the OV threshold, the LFET is turned on again to pull it back down. The condition continues until either the condition forcing OV is removed or the controller is reset by toggling the associated enable pin.

During a VOTF event, the tracking OV and UV thresholds are changed in a manner removing the possibility of nuisance faults. For VOTF up events, the OV threshold is immediately moved to a value related to the final VID voltage. Undervoltage limits remain unchanged until the VOTF up event (plus a settling delay) is completed. For VOTF down events, the UV threshold is immediately moved to a value related to the final VID voltage. Overvoltage limits remain unchanged until the VOTF down event (plus a settling delay) is completed.

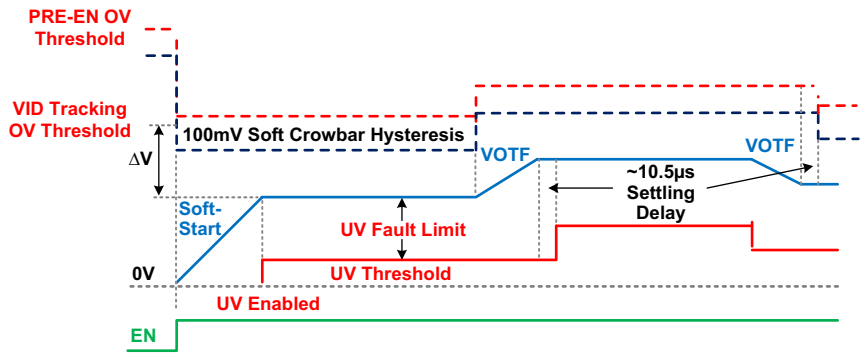


Figure 11. OV/UV Thresholds

6.3 Output Overcurrent Protection

The RAA229620 offers a comprehensive overcurrent protection scheme that monitors the total output current, peak phase current, and the valley phase current. The scheme allows you to eliminate inductor saturation and limit the total output current. The RAA229620 supports shutdown and retry response types for OC faults. The response configuration applies to all output current fault mechanisms such as phase peak overcurrent and total output overcurrent.

Figure 12 shows the block diagram of the output overcurrent protection scheme.

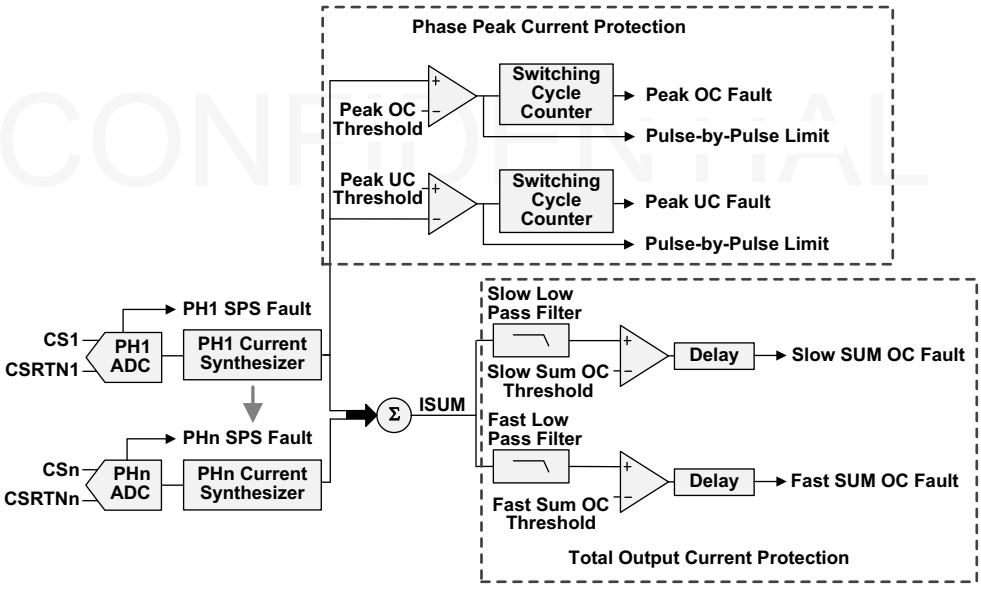


Figure 12. OCP Functional Diagram

Phases are protected from both overcurrent and undercurrent using a pulse-by-pulse scheme that acts instantly on a PWM signal if a detected phase current reaches its threshold. Thresholds for overcurrent and undercurrent allow you to precisely limit phase currents so the inductors never saturate. Phase current limiting behavior can be configured to either shut down the device after a user determined number of consecutive events or continue indefinitely. If configured to continue indefinitely, the converter behaves much like a current source, as Figure 13 and Figure 14 illustrate per-phase current limiting when the device is configured to shut down after a user-determined number of consecutive events.

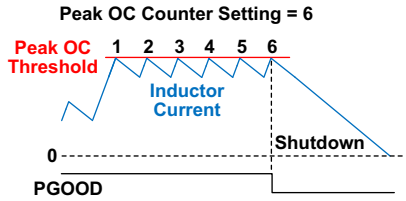


Figure 13. Peak OC Operation

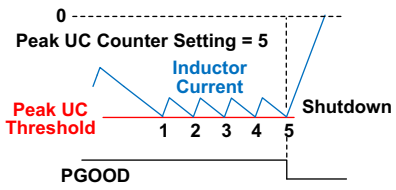


Figure 14. Peak UC Operation

In addition to phase based current limiting, the device supports total output current limits that have user adjustable response delay. The two sum current limits, fast and slow, allow you to permit high maximum output current for a shorter period of time and lower output current for a longer period. The response delay for the limiting mechanisms is also adjustable. These mechanisms do not restrict the maximum output current until the current has exceeded a threshold for the response delay time. For example, suppose the device is configured with a Fast Sum OC limit of 350A, a response delay of 50µs, and a shutdown response type. Next, suppose a 400A load is then placed on the regulator. 400A is supplied to the load for 50µs, and the device then shuts down as shown in Figure 15.

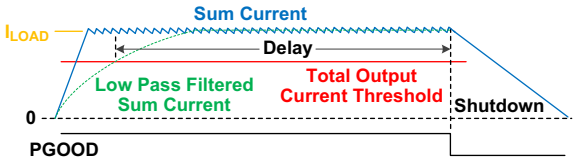


Figure 15. Total Output Current Protection

6.4 Smart Power Stage OC Fault Detect

Renesas Smart Power Stage (SPS) devices output a large signal on their IMON lines if peak current exceeds their preprogrammed threshold; for more details about this functionality, see the relevant SPS datasheet. The RAA229620 detects this fault flag and immediately shuts down by detecting signals that exceed the current-sense ADC full-scale range.

SPS devices that conform to the industry “common footprint”, such as the ISL99380, do not use the IOUT pin for signaling overcurrent faults. All faults are signaled using their TOUT/FLT pins, and the RAA229620 provides a detector on each TEMP pin to support this method.

6.5 Thermal Protection

The RAA229620 supports a comprehensive scheme for thermal alerting and protection. Regardless of temperature sense method, the device supports over or under-temperature faults in addition to over-temperature warning. Temperature faults are triggered based on the hottest reported phase.

IC die temperature is monitored to support telemetry and thermal shutdown. Shutdown occurs at approximately +130°C.

Figure 16 shows the behavior of an over-temperature fault shutdown.

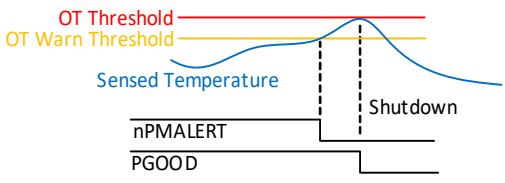


Figure 16. Over-Temperature Shutdown

6.6 Black Box Recorder

Black Box is a powerful diagnostic tool that captures all telemetry and status information when any fault occurs. The RAA229620 continuously monitors all rail and phase information along with the time duration that the rail has been regulating, and the tool captures that data when a fault is registered. Next, the tool reports the first fault bit that occurred to cause the shutdown. This diagnostic data is stored in RAM, and Black Box can be configured to additionally write to NVM for retrieval when the system loses input power upon a fault. The RAM record is updated every time a fault occurs. Black Box can write to NVM up to 10 times and provides an option to limit NVM writing to once per power cycle to avoid filling up the available NVM space inadvertently.

7. AMD SerialVID (SVI3) Interface

The SerialVID (SVI3) Interface circuitry allows an AMD processor to directly control the VDDCR_CPU and VDDCR_SOC voltage reference levels within the RAA229620.

7.1 Rail Assignment

During SVI3 configuration, each rail is assigned a unique address determined by the slave order in the telemetry daisy-chain. The RAA229620 contains two rails and consumes two SVI3 addresses, where Rail 0 is the lower SVI3 address, and Rail 1 is this address plus 1. When SVTI of the RAA229620 is grounded, Rail 1 becomes the terminal slave of the SVI3 bus.

7.2 VOTF Transition

When the outputs are enabled and RESET_L is deasserted, the CPU can begin sending commands through the SVI3 bus, starting with SVI3 bus initialization. The RAA229620 receives the SVI3 VID command and changes the output voltage to the new target at a programmed slew rate. Any telemetry or communication errors that occur are flagged in FAULT_STATUS or NACK_STATUS registers, respectively.

7.3 SVI3 OCP_L

The RAA229620 has a dedicated output pin that supports SVI3 OCP_L functionality. The pin asserts low when the load current exceeds SVI3 OCP_THRESH or OCP_WARN_THRESH.

8. Layout and Design Considerations

The following layout and design strategies help minimize noise coupling and the impact of board parasitic impedances on converter performance, and they optimize the heat dissipating capabilities of the Printed Circuit Board (PCB). Follow these practices during the layout and design process.

8.1 Pin Noise Sensitivity, Design, and Layout Considerations

Table 6 provides general guidance on best practices related to pin noise sensitivity. Use of good engineering judgment is required to implement designs based on criteria specific to the situation.

Table 3. Pin Design and/or Layout Considerations

Pin Name	Noise Sensitive	Description
VINSEN	Yes	Filter VINSEN with 100nF capacitor when sensing VIN directly. Use 10nF when using a resistor divider.
RGNDx VSENx	Yes	Treat each of the remote voltage sense pairs as differential signals in the PCB layout. Route them side by side on the same layer. Do not route them in proximity to noisy signals like PWM or Phase. Place a 3.3nF capacitor across the signals directly at the pins on the top layer.
SVD, SVC, SVTI, SVTO	Yes	**Very Critical!** This is a high speed bus that should be routed carefully to the CPU socket. Provide 20 mils of spacing within SVD, SVT, and SVC, and more than 30 mils to all other signals. See the AMD individual platform design guidelines. A local decoupling capacitor is needed for the pull-up rail.
PGx	No	Open-drain. Avoid connecting pull-up resistor to a rail voltage higher than VCC. Tie to ground when not used.
PMSCL, PMSDA, nPMALERT	Yes	50kHz to 2MHz signals should pair up with nPMALERT and be routed carefully between devices and back to the host. Provide 20 mils of spacing within PMSDA, nPMALERT and PMSCL, and more than 30 mils to all other signals. See the SMBus design guidelines and place proper terminated (pull-up) resistance for impedance matching. Tie to ground when not used. Avoid connecting pull-up resistor to a rail voltage higher than VCC.
TEMPx	Yes	Place a filter capacitor no greater than 500pF between each TEMP pin and ground near the IC. Tie to ground if not used.
VCC	Yes	Place a 1µF MLCC decoupling capacitor (X5R or better) directly at the pin.
VCCS	Yes	Place a 4.7µF MLCC decoupling capacitor (X5R or better) directly at the pin.
PWMx	No	Avoid routing near noise sensitive analog lines such as current sense or voltage sense. Leave floating if not used.
CSx	Yes	Do not route them in close proximity to noisy signals like PWM or Phase. Proper routing of current sense is perhaps the most critical of all the layout tasks.
GND	Yes	This EPAD is the ground for all IC signals. Use four or more vias to directly connect the EPAD to the ground plane. Never use only a single via or a 0Ω resistor connection to the power ground plane. Split ground planes are not advised.
General Comments		The layer next to the top or bottom layer should be a ground layer. The signal layers should be sandwiched between the ground layers if possible.

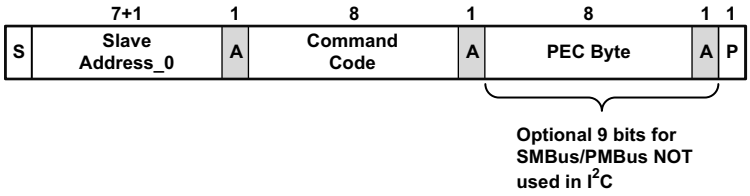
9. PMBus Protocol

The PMBus Protocol includes the Send Byte, the Write Byte/Word, Read Byte/Word, Group Command, and Alert Response Address protocols.

PMBus Protocol Legend

S: Start Condition
A: Acknowledge (“0”)
N: Not Acknowledge (“1”)
W: Write (“0”)
RS: Repeated Start Condition
R: Read (“1”)
PEC: Packet Error Checking
P: Stop Condition
Acknowledge or DATA from Slave, Controller

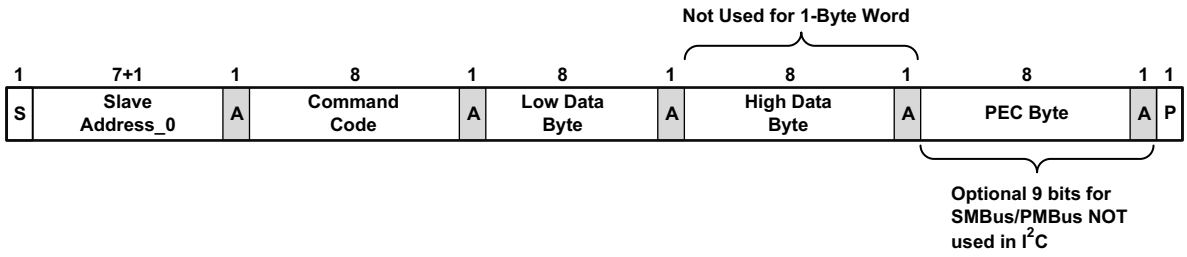
9.1 Send Byte Protocol



Example command: 03h Clear Faults
(This clears all of the bits in Status Byte for the selected rail)

Figure 17. Send Byte Protocol

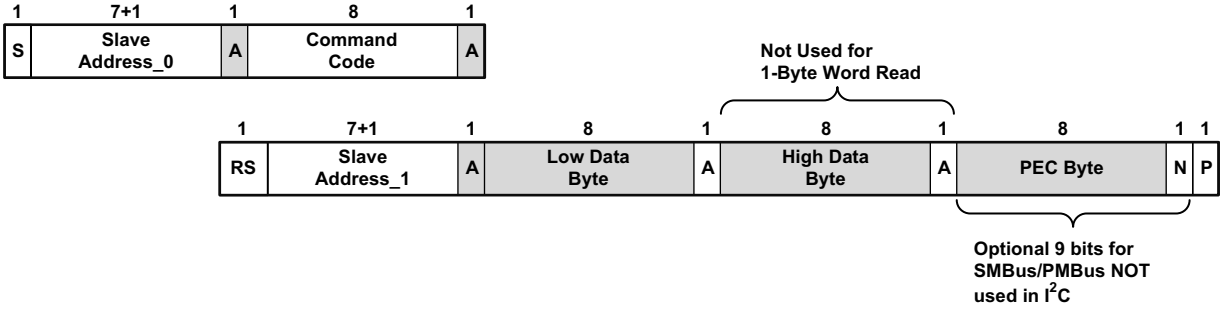
9.2 Write Byte/Word Protocol



Example command: 21h VOUT_COMMAND

Figure 18. Write Byte/Word Protocol

9.3 Read Byte/Word Protocol

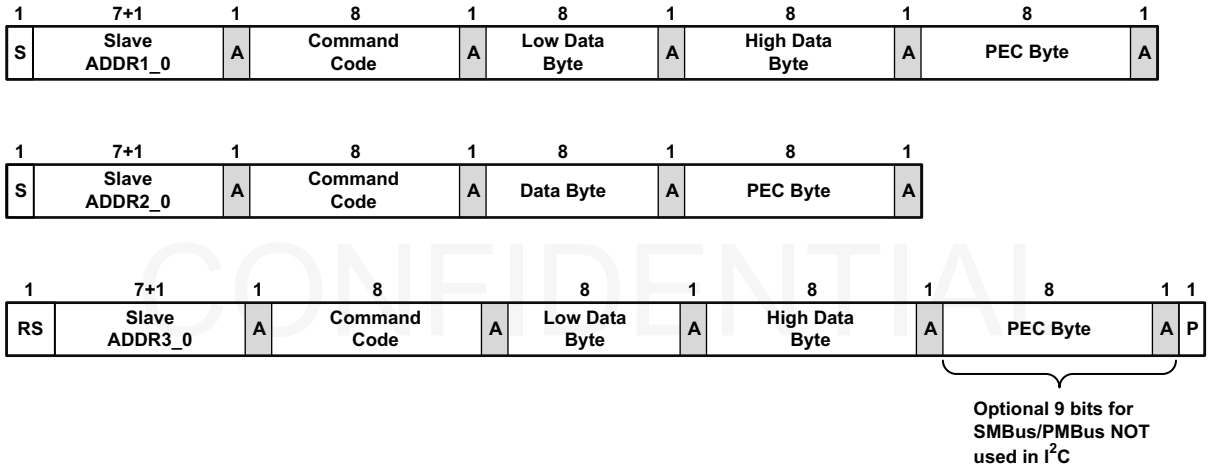


Example command: 8B READ_VOUT (Two words, read voltage of the selected rail).

Note: The STOP (P) bit is NOT allowed before the repeated START condition when reading contents of a register.

Figure 19. Read Byte/Word Protocol

9.4 Group Command Protocol



Note: No more than one command can be sent to the same Address

Figure 20. Group Command Protocol

9.5 Alert Response Address

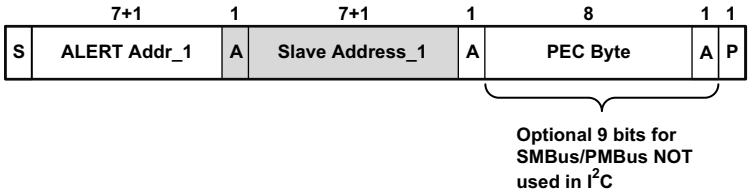


Figure 21. Alert Response Address (ARA, 0001_1001, 25h) for SMBus and PMBus, not used for I^2C

10. PMBus Summary Commands

Code	Command Name	Description	Type	Data Format	Default Value	Default Setting
00h	PAGE (00h)	Rail selector	R/W	Bit	00h	Page 0
01h	OPERATION (01h)	Enable/disable, V_{OUT} source	R/W	Bit	08h	Immediate off
02h	ON_OFF_CONFIG (02h)	On/off configuration settings	R/W	Bit	17h	ENABLE pin control, active high
03h	CLEAR_FAULTS (03h)	Clears all fault bits in all registers and releases the nPMALERT pin	Write	N/A	N/A	N/A
04h	PHASE (04h)	Phase selector	R/W	Direct	00h	Phase 0
05h	PAGE_PLUS_WRITE (05h)	Allows page and command write in single transaction	Block Write	N/A	N/A	N/A
06h	PAGE_PLUS_READ (06h)	Allows page and command read in single transaction	Block Write/Read/ process call	N/A	N/A	N/A
10h	WRITE_PROTECT (10h)	Write protection to sets of commands	R/W	Bit	00h	No write protection
19h	CAPABILITY (19h)	Reports PMBus capability	Read	Bit	D0h	See detail
1Bh	SMBALERT_MASK (1Bh)	Mask status bits from SMBALERT signal	Block R/W	Bit	00h	No bits masked
20h	VOUT_MODE (20h)	Defines format for output voltage related commands	Read	Bit	40h	Direct format
21h	VOUT_COMMAND (21h)	Output voltage set by PMBus	R/W	Direct	0384h	900mV
22h	VOUT_TRIM (22h)	Applies trim voltage to V_{OUT} set-point	R/W	Direct	0000h	0mV
23h	VOUT_CAL_OFFSET (23h)	Applies offset voltage to V_{OUT} set-point	R/W	Direct	0000h	0mV
24h	VOUT_MAX (24h)	Absolute maximum voltage setting	R/W	Direct	0BEAh	3050mV
25h	VOUT_MARGIN_HIGH (25h)	Sets voltage target during margin high	R/W	Direct	03B1h	945mV
26h	VOUT_MARGIN_LOW (26h)	Sets voltage target during margin low	R/W	Direct	0357h	855mV
27h	VOUT_TRANSITION_RATE (27h)	Slew rate setting for V_{OUT} ramp	R/W	Direct	09C4h	25mV/µs
28h	VOUT_DROOP (28h)	Sets the load-line (V/I slope) resistance for the output	R/W	Direct	0000h	0µV/A

Code	Command Name	Description	Type	Data Format	Default Value	Default Setting
2Bh	VOUT_MIN (2Bh)	Absolute minimum voltage setting	R/W	Direct	0000h	0mV
33h	FREQUENCY_SWITCH (33h)	Sets PWM switching frequency	R/W	Direct	0258h	600khz
35h	VIN_ON (35h)	Sets the V_{IN} startup threshold	R/W	Direct	02BCh	7000mV
36h	VIN_OFF (36h)	Sets the V_{IN} shutdown threshold	R/W	Direct	01F4h	5000mV
40h	VOUT_OV_FAULT_LIMIT (40h)	Sets the V_{OUT} OV fault limit while disabled	R/W	Direct	0C1Ch	3100mV
41h	VOUT_OV_FAULT_RESPONSE (41h)	Configures the V_{OUT} OV fault response	R/W	Bit	84h	Latch off
45h	VOUT_UV_FAULT_RESPONSE (45h)	Configures the V_{OUT} UV fault response	R/W	Bit	84h	Latch off
46h	IOUT_OC_FAULT_LIMIT (46h)	Sets the I_{OUT} OC fault limit	R/W	Direct	012Ch	30A
47h	IOUT_OC_FAULT_RESPONSE (47h)	Configures the I_{OUT} OC fault response	R/W	Bit	C4h	Latch off
4Ah	IOUT_OC_WARN_LIMIT (4Ah)	Sets the I_{OUT} OC warn limit	R/W	Direct	TBD	TBD
4Fh	IOUT_OC_WARN_LIMIT (4Ah)	Sets the OT fault limit	R/W	Direct	007Dh	125°C
50h	OT_FAULT_RESPONSE (50h)	Configures the OT fault response	R/W	Bit	84h	Latch off
51h	OT_WARN_LIMIT (51h)	Sets the OT warn limit	R/W	Direct	006Eh	110°C
53h	UT_FAULT_LIMIT (53h)	Sets the UT fault limit	R/W	Direct	FFD8h	-40°C
54h	UT_FAULT_RESPONSE (54h)	Configures the UT fault response	R/W	Bit	84h	Latch off
55h	VIN_OV_FAULT_LIMIT (55h)	Sets the V_{IN} OV fault limit	R/W	Direct	0640h	16000mV
56h	VIN_OV_FAULT_RESPONSE (56h)	Configures the V_{IN} OV fault response	R/W	Bit	84h	Latch off
57h	VIN_OV_WARN_LIMIT (57h)	Sets the VIN OV warn limit	R/W	Direct	0708h	18000mV
58h	VIN_UV_WARN_LIMIT (58h)	Sets the VIN UV warn limit	R/W	Direct	0000h	0mV
59h	VIN_UV_FAULT_LIMIT (59h)	Sets the V_{IN} UV fault limit	R/W	Direct	0000h	0mV
5Ah	VIN_UV_FAULT_RESPONSE (5Ah)	Configures the V_{IN} UV fault response	R/W	Bit	84h	Ignore
5Bh	IIN_OC_FAULT_LIMIT (5Bh)	Sets the I_{IN} OC fault limit	R/W	Direct	3A98h	150A
5Ch	IIN_OC_FAULT_RESPONSE (5Ch)	Configures the I_{IN} OC fault response	R/W	Bit	04h	Ignore
5Dh	IIN_OC_WARN_LIMIT (5Dh)	Sets the I_{IN} OC warn limit	R/W	Direct	3A98h	150A

Code	Command Name	Description	Type	Data Format	Default Value	Default Setting
60h	TON_DELAY (60h)	Sets turn on delay time	R/W	Direct	0000h	0µs
61h	TON_RISE (61h)	Sets turn on rise time	R/W	Direct	0032h	500µs
64h	TOFF_DELAY (64h)	Sets turn off delay time	R/W	Direct	0000h	0µs
65h	TOFF_FALL (65h)	Sets turn off fall time	R/W	Direct	0032h	500µs
78h	STATUS_BYTE (78h)	First byte of STATUS_WORD	Read	Bit	N/A	N/A
79h	STATUS_WORD (79h)	Summary of critical faults	Read	Bit	N/A	N/A
7Ah	STATUS_VOUT (7Ah)	Reports V_{OUT} warnings/faults	Read	Bit	N/A	N/A
7Bh	STATUS_IOUT (7Bh)	Reports I_{OUT} warnings/faults	Read	Bit	N/A	N/A
7Ch	STATUS_INPUT (7Ch)	Reports input warnings/faults	Read	Bit	N/A	N/A
7Dh	STATUS_TEMPERATURE (7Dh)	Reports temperature warnings/faults	Read	Bit	N/A	N/A
7Eh	STATUS_CML (7Eh)	Reports communication, memory, logic errors	Read	Bit	N/A	N/A
80h	STATUS_MFR_SPECIFIC (80h)	Reports other specific faults	Read	Bit	N/A	N/A
88h	READ_VIN (88h)	Reports input voltage measurement	Read	Direct	N/A	N/A
89h	READ_IIN (89h)	Reports input current measurement	Read	Direct	N/A	N/A
8Bh	READ_VOUT (8Bh)	Reports output voltage measurement	Read	Direct	N/A	N/A
8Ch	READ_IOUT (8Ch)	Reports output current measurement	Read	Direct	N/A	N/A
8Dh	READ_TEMPERATURE_1 (8Dh)	Reports power stage temperature measurement	Read	Direct	N/A	N/A
8Eh	READ_TEMPERATURE_2 (8Eh)	Reports internal temperature measurement	Read	Direct	N/A	N/A
96h	READ_POUT (96h)	Reports output power	Read	Direct	N/A	N/A
97h	READ_PIN (97h)	Reports input power	Read	Direct	N/A	N/A
98h	PMBUS_REVISION (98h)	Reports the PMBus revision used	Read	Bit	33h	P1 R1.3, P2 R1.3
99h	MFR_ID (99h)	Stores Inventory Information	Block R/W	Bit	00000000h	Nothing stored
9Ah	MFR_MODEL (9Ah)	Stores Inventory Information	Block R/W	Bit	00000000h	Nothing stored
9Bh	MFR_REVISION (9Bh)	Stores Inventory Information	Block R/W	Bit	00000000h	Nothing stored

Code	Command Name	Description	Type	Data Format	Default Value	Default Setting
9Dh	MFR_DATE (9Dh)	Stores Inventory Information	Block R/W	Bit	00000000h	Nothing stored
ADh	IC_DEVICE_ID (ADh)	Reports device identification information	Block Read	Bit	49D28B00h	RAA229620
AEh	IC_DEVICE_REV (AEh)	Reports device revision information	Block Read	Bit	N/A	Release revision
C5h	DMAFIX (C5h)	Fixed DMA transactions	R/W	Bit	N/A	N/A
C6h	DMASEQ (C6h)	Sequential DMA transaction	R/W	Bit	N/A	N/A
C7h	DMAADDR (C7h)	Sets the address for DMA transactions	R/W	Bit	N/A	N/A
C8h	READ_VMON_IINSEN (C8h)	Reports VMON/IINSEN pin telemetry	Read	Direct	N/A	N/A
CCh	READ_VMON_IINSEN (C8h)	Alternate boot ramp rate	R/W	Direct	01F4h	5000µV/µs
CDh	PEAK_OC_LIMIT (CDh)	Sets peak per phase OC limit	R/W	Direct	0258h	60A
CEh	PEAK_UC_LIMIT (CEh)	Sets peak per phase UC limit	R/W	Direct	FDA8h	-60A
D0h	VMON_ON (D0h)	Sets the VMON startup threshold	R/W	Direct	01C2h	4500mV
D1h	VMON_OFF (D1h)	Sets the VMON shutdown threshold	R/W	Direct	0190h	4000mV
DDh	VMON_ON (D0h)	Configures proportional gain	R/W	Bit	D90907C4h	See Detail
DEh	COMPINTEG (DEh)	Configures integral gain	R/W	Bit	000000A9h	See Detail
DFh	COMPDIFF (DFh)	Configures differential gain	R/W	Bit	0000h	See Detail
E0h	COMPCFB (E0h)	Configures AC current feedback	R/W	Bit	0560h	See Detail
E3h	HS_BUS_CURRENT_SCALE (E3h)	Sets the high speed bus current scaling	R/W	Direct	4000h	1.0
E4h	PHASE_CURRENT (E4h)	Reports per-phase current	Read	Direct	N/A	N/A
E9h	PEAK_OCUC_COUNT (E9h)	Sets the count limit before fault	R/W	Bit	0606h	6 cycles OC and UC
EAh	SLOW_IOUT_OC_LIMIT (EAh)	Sets the slow I_{OUT} OC limit	R/W	Direct	00C8h	20A
EBh	FAST_OC_FILT_COUNT (EBh)	Configures the fast OC filter	R/W	Bit	0696h	See Detail
ECh	SLOW_OC_FILT_COUNT (ECh)	Configures the slow OC filter	R/W	Bit	0606h	See Detail

Code	Command Name	Description	Type	Data Format	Default Value	Default Setting
F0h	LOOPCFG (F0h)	Defines loop operating configuration	R/W	Bit	102071F6h	See Detail
F2h	RESTORE_CFG (F2h)	Identifies configuration to be restored from NVM	R/W	Bit	00h	N/A

10.1 PMBus Data Formats

10.1.1 Direct

The Direct data format is a 2-byte binary integer.

10.1.2 Linear 16 Unsigned (L16U)

The L16u data format uses a fixed exponent (hard-coded to N = -9h) and a 16-bit unsigned integer mantissa (Y) to represent the real world decimal value (X). The relation between the real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-9}$.

10.1.3 Linear 16 Signed (L16S)

The L16S data format uses a fixed exponent (hard-coded to N = -9h) and a 16-bit signed integer mantissa (Y) to represent the real world decimal value (X). The relation between the real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-9}$.

10.1.4 Linear 11 (L11)

The L11 data format uses a 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent the real world decimal value (X).

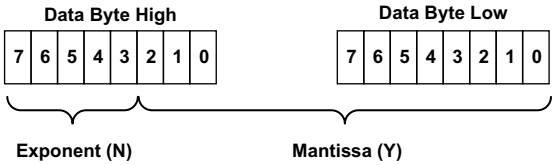


Figure 22. Linear 11 Data Format

The relation between the real world decimal value (X), N, and Y is: $X = Y \cdot 2^{N}$.

10.1.5 Bit Field (Bit)

A description of Bit Field is provided in the PMBus Command Detail.

10.1.6 Custom (Cus)

Custom format

11. PMBus Command Detail

11.1 PAGE (00h)

Definition: Selects the communication path to rail 0, rail 1, both rails, or individual phases. All paged commands following this command are received and acted on by the selected destination path. Paged commands that can be written can be written globally, but can only be read on a specific page unless otherwise specified. Global commands remain global regardless of the value of this command. Individual phase access is available by setting this command to 80h and setting the individual phase value using the PHASE command.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 00h

Command	PAGE (00h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bit Value	Setting
00h	Page 0 (Rail 0)
01h	Page 1 (Rail 1)
80h	Individual Phase (set by the PHASE command)
FFh	Global (All Rails)

11.2 OPERATION (01h)

Definition: Sets Enable state when configured for PMBus enable. Sets the source of the V_{OUT} setting when LOCKSVID is configured for PMBus override.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 08h (Immediate off)

Command	OPERATION (01h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Purpose	Bit Value	Meaning
7	Enable/Disable Output	0	Disable
		1	Enable
6	Disable Behavior	0	Immediate off (decay)
		1	Soft off (Use TOFF_DELAY and TOFF_FALL)
5:4	V_{OUT} Source	00	VOUT_COMMAND
		01	VOUT_MARGIN_LOW
		10	VOUT_MARGIN_HIGH
		11	Not used
3:2	Margin Response	01	Ignore V_{OUT} OV, UV Faults when margined
		10	Act on V_{OUT} OV, UV Faults when margined
1:0	Not Supported	XX	Not supported

11.3 ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 17h (ENABLE pin control)

Command	ON_OFF_CONFIG (02h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	1	0	1	1	0

Bit Number	Purpose	Bit Value	Meaning
7:5	Not Supported	000	Not supported
4:2	Sets the source of enable	0XX	Output enables any time power is present regardless of pin or OPERATION command state.
		101	Output enables from the enable pin only
		110	Output enables from the OPERATION command only
		111	Output enables from the enable pin AND the OPERATION command. Both must be set to enable.
1	Polarity of ENABLE pin	0	Active low
		1	Active high
0	ENABLE pin action when commanding the unit to turn off	0	Use the configured TOFF_DELAY and TOFF_FALL settings.
		1	Turn off the output immediately with decay.

11.4 CLEAR_FAULTS (03h)

Definition: Clears all fault status bits in all registers and releases the nPMALERT pin (if asserted) simultaneously. If a fault condition still exists, the bit(s) reasserts immediately. This command does not restart a device if it is shut down, it only clears the faults.

Access: Paged

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

11.5 PHASE (04h)

Definition: Sets the individual phase address for reading from PHASE_CURRENT (E4h). The PAGE command must also be set to access phase information.

Access: Global

Data Length in Bytes: 1

Data Format: Direct

Type: R/W

Default Value: 00h (phase 0)

Equation: PHASE = (direct value)

Range: Phase 0 to 7

Command	PHASE (04h)							
Format	Direct							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer							
Default Value	0	0	0	0	0	0	0	0

11.6 PAGE_PLUS_WRITE (05h)

Definition: Sets the page within a device, send a command, and send the data for the command in one packet.

Access: Global

Data Format: Bit Field

Type: Block Write

The PAGE_PLUS_WRITE command uses the WRITE BLOCK protocol.

An example of the PAGE_PLUS command sending a command that has two data bytes to be written and a PEC byte is shown in Figure 23.

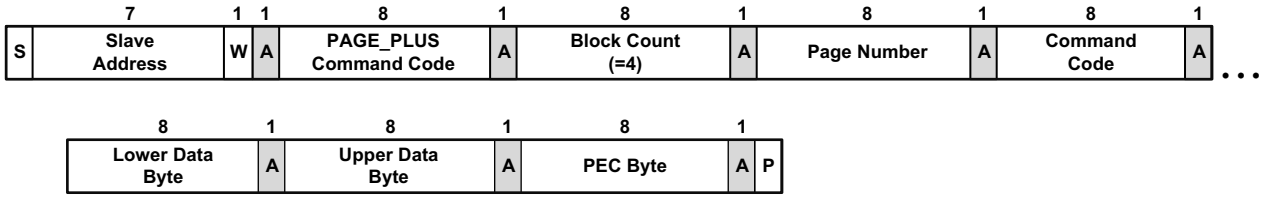


Figure 23. PAGE_PLUS_WRITE Command with a PEC Byte

11.7 PAGE_PLUS_READ (06h)

Definition: Sets the page within a device, send a command, and read the data returned by the command in one packet.

Access: Paged

Data Format: Bit Field

Type: Block Read

The PAGE_PLUS_READ command uses the BLOCK WRITE – BLOCK READ PROCESS CALL protocol.

An example of the PAGE_PLUS command sending a command that has two data bytes to be read and a PEC byte is shown in Figure 24.

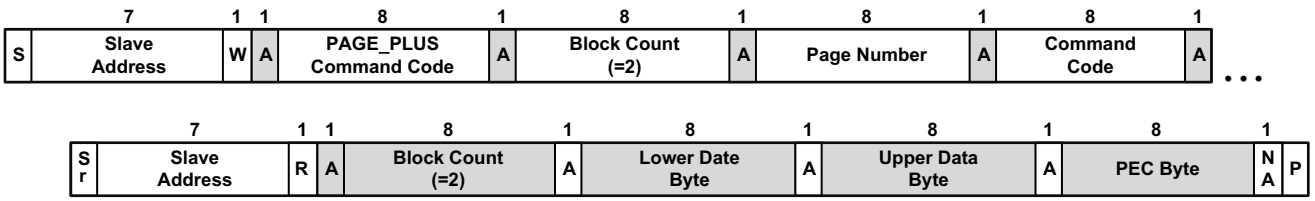


Figure 24. PAGE_PLUS_READ Command with a PEC Byte

11.8 WRITE_PROTECT (10h)

Definition: Sets the write protection of certain configuration commands.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 00h (enable all writes)

Command	WRITE_PROTECT (10h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bits 7:0	Protection
1000 0000	Disable all writes except to WRITE_PROTECT command.
0100 0000	Disable all writes except to WRITE_PROTECT, OPERATION, and PAGE.
0010 0000	Disable all writes except to WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND.
0000 0010	Disable all writes except to WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, VOUT_COMMAND and DMA.
0000 0000	Enable all writes
Note: Any settings other than the five shown in the table results in an invalid data fault.	

11.9 CAPABILITY (19h)

Definition: Reports PMBus capabilities of the device.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: D0h (PEC supported, bus speed 1MHz, SMBALERT supported, Linear/Direct numeric data)

Command	CAPABILITY (19h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	1	1	0	1	0	0	0	0

Bit Number	Purpose	Bit Value	Meaning
7	PEC Support	1	PEC supported
		0	PEC not supported
6:5	Maximum Bus Speed	11	Not supported
		10	1MHz
		01	400kHz
		00	100kHz
4	SMBALERT Support	1	SMBALERT pin and response protocol is supported.
		0	SMBALERT pin and response protocol is not supported.
3	Numeric Format	1	Numeric data, IEEE half precision floating point format
		0	Numeric data, Linear/Direct
2	AVSBus Support	1	AVSBus supported
		0	AVSBus not supported
1:0	Not Supported	00	Not supported

11.10 SMBALERT_MASK (1Bh)

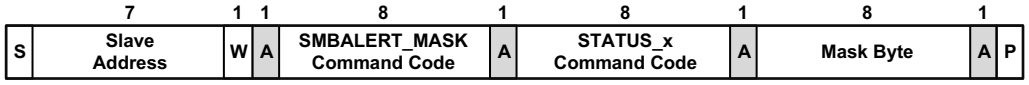
Definition: Prevents a warning or fault condition from asserting the SMBALERT# signal. Can be used on the following PMBus status commands: STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML, and STATUS_MFR_SPECIFIC.

Access: Paged

Data Format: Bit Field

Type: Block R/W

The command format that blocks a status bit or bits from causing the SMBALERT# signal to be asserted is shown in Figure 25 and Figure 26. The bits in the mask byte align with the bits in the corresponding status register. For example if the STATUS_TEMPERATURE command code were sent with the mask byte 01000000b, then an over-temperature warning condition would be blocked from asserting SMBALERT#.



Note: The figure shows the command format used by the host to determine the SMBALERT_MASK setting for a given status register.

Figure 25. SMBALERT_MASK Command Packet Format

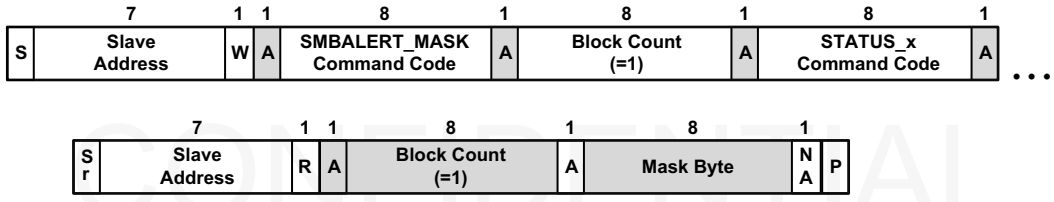


Figure 26. Retrieving the SMBALERT_MASK Setting for a Given Status Register

11.11 VOUT_MODE (20h)

Definition: Returns the supported V_{OUT} mode. Direct mode, 1mV per LSB.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: 40h

Command	VOUT_MODE (20h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mode			Exponent				
Default Value	0	1	0	0	0	0	0	0

11.12 VOUT_COMMAND (21h)

Definition: Sets the value of V_{OUT} when the OPERATION command is configured for PMBus nominal operation and Lock SVID is configured for PMBus override. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0384h (900mV)

Units: mV

Equation: V_{OUT} Command = (Direct value)

Range: 0mV to 3050mV

Command	VOUT_COMMAND (21h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0

11.13 VOUT_TRIM (22h)

Definition: Applies a fixed trim voltage to the output voltage command value when Lock SVID is configured for PMBus override. This command typically calibrates a device in the application circuit. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0mV)

Units: mV

Equation: V_{OUT} Trim = (Direct value)

Range: Any value that results in the V_{OUT} target being between 0V and VOUT_MAX

Command	VOUT_TRIM (22h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.14 VOUT_CAL_OFFSET (23h)

Definition: Applies a fixed offset voltage to the output voltage command value. This command typically calibrates a device in the application circuit. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0mV)

Units: mV

Equation: V_{OUT} Cal Offset = (Direct value)

Range: Any value that results in the V_{OUT} target being between 0V and VOUT_MAX

Command	VOUT_CAL_OFFSET (23h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.15 VOUT_MAX (24h)

Definition: Sets the absolute maximum V_{OUT} regulation value regardless of any other commands or combinations. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0BEAh (3050mV)

Units: mV

Equation: V_{OUT} Max = (Direct value)

Range: 0mV to 3050mV

Command	VOUT_MAX (24h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	1	0	0	0	1	1	1	1	1	1	0	0

11.16 VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of V_{OUT} when the OPERATION command is configured for margin high. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 03B1h (945mV)

Units: mV

Equation: V_{OUT} Margin High = (Direct value)

Range: 0mV to 3050mV

Command	VOUT_MARGIN_HIGH (25h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0

11.17 VOUT_MARGIN_LOW (26h)

Definition: Sets the value of V_{OUT} when the OPERATION command is configured for margin low. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0357h (855mV)

Units: mV

Equation: V_{OUT} Margin Low = (Direct value)

Range: 0mV to 3050mV

Command	VOUT_MARGIN_LOW (26h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0

11.18 VOUT_TRANSITION_RATE (27h)

Definition: Defines the output voltage rate of change during regulation. 0.01mV/µs per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 09C4h (25mV/µs)

Units: mV/µs

Equation: V_{OUT} Transition Rate = (Direct value)/100

Range: 10µV/µs to 100mV/µs

Command	VOUT_TRANSITION_RATE (27h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.19 VOUT_DROOP (28h)

Definition: Sets the rate at which output voltage changes relative to output current during regulation. 10µV/A per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0µV/A)

Units: µV/A

Equation: V_{OUT} Droop = (Direct value) * 10

Range: 0µV/A to 16000µV/A

Command	VOUT_DROOP (28h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.20 VOUT_MIN (2Bh)

Definition: Sets the absolute minimum voltage that is delivered to the output during regulation. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0mV)

Units: mV

Equation: V_{OUT} Min = (Direct value)

Range: 0mV to 3050mV

Command	VOUT_MIN (2Bh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.21 FREQUENCY_SWITCH (33h)

Definition: Sets the PWM switching frequency during regulation. 1kHz per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0258h (600kHz)

Units: kHz

Equation: Frequency Switch = (Direct value)

Range: 200kHz to 2MHz

Command	FREQUENCY-SWITCH (33h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.22 VIN_ON (35h)

Definition: Sets the input voltage rising threshold at which the output can be enabled. 10mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 02BCh (7000mV)

Units: mV

Equation: V_{IN} On = (Direct value)*10

Range: -327680mV to 327670mV

Command	VIN_ON (35h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	1	1	0	1	1	0	1	0	1	1	0	0	0	0

11.23 VIN_OFF (36h)

Definition: Sets the input voltage falling threshold at which the output disables. 10mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 01F4h (5,000mV)

Units: mV

Equation: V_{IN} Off = (Direct value) *10

Range: -327680mV to 327670mV

Command	VIN_OFF (36h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	1	1	0	1	1	0	1	0	1	1	0	0	0	0

11.24 VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the disabled rail overvoltage threshold for crowbar function, should be set above any programmed voltage target. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0C1Ch (3100mV)

Units: mV

Equation: V_{OUT} OV Fault Limit = (Direct value)

Range: 0mV to 3050mV

Command	VOUT_OV_FAULT_LIMIT (40h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	1	1	1	0	1	1	0	1	1	0	0

11.25 VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the output overvoltage fault response. For a fault to be considered cleared, the output must drop by 100mV.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

Command	VOUT_OV_FAULT_RESPONSE (41h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

Bit	Field Name	Value	Description
7:6	Response Behavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption
		01	Not supported
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not supported
5:3	Retry Setting	000	No retry. The output remains disabled until the rail is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	0ms delay (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.26 VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the output undervoltage fault response. This fault is masked during ramp or when disabled.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

Command	VOUT_UV_FAULT_RESPONSE (45h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

Bit	Field Name	Value	Description
7:6	ResponseBehavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption
		01	Not supported
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not supported
5:3	Retry Setting	000	No retry. The output remains disabled until the rail is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.27 IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the fast sum output overcurrent fault threshold. 0.1A per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 012Ch (30A)

Units: A

Equation: I_{OUT} OC Fault Limit = (Direct value)/10

Range: 0A to 3276.7A

Command	IOUT_OC_FAULT_LIMIT (46h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.28 IOUT_OC_FAULT_RESPONSE (47h)

Definition: Configures the output overcurrent fault response for all I_{OUT} OC detection methods. This response setting is also applied to output undercurrent faults.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: C4h (latch off)

Command	IOUT_OC_FAULT_RESPONSE (47h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	1	0	0	0	0	0	0

Bit	Field Name	Value	Description
7:6	ResponseBehavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption
		01-10	Not supported
		11	Disable and retry as set in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the rail is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.29 IOUT_OC_WARN_LIMIT (4Ah)

Definition: Sets the fast sum output overcurrent warn threshold. 0.1A per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: TBD

Units: A

Equation: I_{OUT} OC Warn Limit = (Direct value)/10

Range: 0A to 3276.7A

Command	IOUT_OC_WARN_LIMIT (4Ah)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.30 OT_FAULT_LIMIT (4Fh)

Definition: Sets the power stage over-temperature fault limit. 1°C per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 007Dh (125°C)

Units: °C

Equation: OT Fault Limit = (Direct value)

Range: 0°C to +150°C

Command	OT_FAULT_LIMIT (4Fh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

11.31 OT_FAULT_RESPONSE (50h)

Definition: Configures the power stage over-temperature fault response. For a fault to be considered cleared, the temperature must drop 5°C below the OT fault threshold value.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

Command	OT_FAULT_RESPONSE (50h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

Bit	Field Name	Value	Description
7:6	ResponseBehavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption
		01	Not supported
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not supported
5:3	Retry Setting	000	No retry. The output remains disabled until the rail is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.32 OT_WARN_LIMIT (51h)

Definition: Sets the power stage over temperature warn limit. 1°C per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 006Eh (110°C)

Units: °C

Equation: OT Warn Limit = (Direct value)

Range: 0°C to 150°C

Command	OT_WARN_LIMIT (51h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0

11.33 UT_FAULT_LIMIT (53h)

Definition: Sets the power stage under-temperature fault limit. 1°C per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: FFD8h (-40°C)

Units: °C

Equation: UT Fault Limit = (Direct value)

Range: -50°C to 150°C

Command	UT_FAULT_LIMIT (53h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	0

11.34 UT_FAULT_RESPONSE (54h)

Definition: Configures the power stage under-temperature fault response. For the fault to be considered cleared, the temperature must rise 5°C above the UT fault threshold value.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

Command	UT_FAULT_RESPONSE (54h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

Bit	Field Name	Value	Description
7:6	ResponseBehavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption
		01	Not supported
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not supported
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.35 VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold. 10mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0640h (16,000mV)

Units: mV

Equation: V_{IN} OV Fault Limit = (Direct value) *10

Range: -327680mV to 327670mV

Command	VIN_OV_FAULT_LIMIT (55h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	1	1	0	1	1	0	1	0	1	1	0	0	0	0

11.36 VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the input overvoltage fault response. For a fault to be considered cleared, the input voltage must drop by 1/16th of the OV fault threshold value.

Access: Paged

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 84h (latch off)

Command	VIN_OV_FAULT_RESPONSE (56h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

Bit	Field Name	Value	Description
7:6	ResponseBehavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption
		01	Not supported
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not supported
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.37 VIN_OV_WARN_LIMIT (57h)

Definition: Sets the V_{IN} over voltage warning threshold. 10mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0708h (18,000mV)

Units: mV

Equation: V_{IN} OV Warn Limit = (Direct value) *10

Range: -327680mV to 327670mV

Command	VIN_OV_WARN_LIMIT (57h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0

11.38 VIN_UV_WARN_LIMIT (58h)

Definition: Sets the V_{IN} under voltage warning threshold. 10mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0mV)

Units: mV

Equation: Vin UV Warn Limit = (Direct value) *10

Range: -327680mV to 327670mV

Command	VIN_UV_WARN_LIMIT (58h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.39 VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold. 10mV per LSB. If using VIN_ON and VIN_OFF commands, this command should be set to 0V.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0mV)

Units: mV

Equation: V_{IN} UV Fault Limit = (Direct value) *10

Range: -327680mV to 327670mV

Command	VIN_UV_FAULT_LIMIT (59h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.40 VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the input undervoltage fault response. For a fault to be considered cleared, the input voltage must rise by 1/16th of the UV fault threshold value.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

Command	VIN_UV_FAULT_RESPONSE (5Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

Bit	Field Name	Value	Description
7:6	ResponseBehavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption
		01	Not supported
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not supported
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.41 IIN_OC_FAULT_LIMIT (5Bh)

Definition: Sets the input overcurrent fault threshold for the synthesized input current reading at READ_IIN. 10mA per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 3A98h (150A)

Units: A

Equation: I_{IN} OC Fault Limit = (Direct value)/100

Range: -327.68A to 327.67A

Command	IIN_OC_FAULT_LIMIT (5Bh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

11.42 IIN_OC_FAULT_RESPONSE (5Ch)

Definition: Configures the input overcurrent fault response for the synthesized input current reading at READ_IIN.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 04h (ignore)

Command	IIN_OC_FAULT_RESPONSE (5Ch)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	1	0	0	0	0	0	0

Bit	Field Name	Value	Description
7:6	ResponseBehavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption
		01-10	Not supported
		11	Disable and retry as set in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.43 IIN_OC_WARN_LIMIT (5Dh)

Definition: Sets the input over current warn threshold. 10mA per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 3A98h (150A)

Units: A

Equation: I_{IN} OC Warn Limit = (Direct value)/100

Range: -327.68A to 327.67A

Command	IIN_OC_WARN_LIMIT (5Dh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0

11.44 TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise. Values smaller than 80µs result in the controller starting when it is ready. 10µs per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0µs)

Units: µs

Equation: t_{ON}Delay = (Direct value) * 10

Range: -327.68A to 327.67A

Command	TON_DELAY (60h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.45 TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} during enable. 1µs per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0032h (500µs)

Units: µs

Equation: t_{ON} Rise = (Direct value)

Range: 0µs to 10000µs

Command	TON_RISE (61h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.46 TOFF_DELAY (64h)

Definition: Sets the delay time of V_{OUT} during disable when configured for soft off. 10µs per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0µs)

Units: µs

Equation: t_{OFF} Delay = (Direct value)*10

Range: 0µs to 655534µs

Command	TOFF_DELAY (64h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.47 TOFF_FALL (65h)

Definition: Sets the fall time of V_{OUT} during disable when configured for soft off. 1µs per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0032h (500µs)

Units: µs

Equation: t_{OFF} Fall = (Direct value)

Range: 0µs to 10000µs

Command	TOFF_FALL (65h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.48 STATUS_BYTE (78h)

Definition: Returns a summary of the device status. Based on the information in this byte, the host can get more information by reading the appropriate status registers. Depending on the setting of the PAGE command, this command returns information about individual rails or a global summary of all rail statuses.

Access: Paged and Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Command	STATUS_BYTE (78h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit Number	Status Bit Name	Meaning
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	None of the Above	A fault other than those listed above has occurred.

11.49 STATUS_WORD (79h)

Definition: Returns a summary of the device status. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. Depending on the setting of the PAGE command, this command returns information about individual rails or a global summary of all rail statuses. The low byte of the STATUS_WORD is the same as the STATUS_BYTE (78h) command.

Access: Paged and Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Command	STATUS_WORD (79h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															

Bit Number	Status Bit Name	Meaning
15	V_{OUT}	An output voltage fault or warning has occurred.
14	I_{OUT}	An output current fault has occurred.
13	INPUT	An input voltage fault or warning has occurred.
12	MFR_SPECIFIC	A manufacturer specific fault or warning has occurred.
11	POWER_GOOD #	The POWER_GOOD signal is negated.[1]
10:9	Not Supported	Not supported
8	Unknown	A fault other than those described in Bits 15:9 has occurred.
7	Busy	Device busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	None of the Above	A status change other than those listed above has occurred.

1. If the POWER_GOOD# Bit is set, this indicates that the POWER_GOOD signal is signaling that the output power is not good.

11.50 STATUS_VOUT (7Ah)

Definition: Returns a summary of output voltage status.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Command	STATUS_VOUT (7Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit Number	Status Bit Name	Meaning
7	VOUT_OV_FAULT	Indicates an output overvoltage fault has occurred.
6:5	Not Supported	Not supported
4	VOUT_UV_FAULT	Indicates an output undervoltage fault has occurred.
3	VOUT_MAX Warning	Indicates an output voltage maximum warning has occurred.
2:0	Not Supported	Not supported

11.51 STATUS_IOUT (7Bh)

Definition: Returns a summary of output current status.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Command	STATUS_IOUT (7Bh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit Number	Status Bit Name	Meaning
7	IOUT_OC_FAULT	An output overcurrent fault has occurred.
6	Not Supported	Not supported
5	IOUT_OC_WARN	An output overcurrent warning has occurred.
4	IOUT_UC_FAULT	An output undercurrent fault has occurred.

Bit Number	Status Bit Name	Meaning
3	Current Share Fault	A current share fault has occurred.
2:0	Not Supported	Not supported

11.52 STATUS_INPUT (7Ch)

Definition: Returns a summary of input status.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Command	STATUS_INPUT (7Ch)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit Number	Status Bit Name	Meaning
7	VIN_OV_FAULT	An input overvoltage fault has occurred.
6	VIN_OV_WARN	An input overvoltage warning has occurred.
5	VIN_UV_WARN	An input undervoltage warning has occurred.
4	VIN_UV_FAULT	An input undervoltage fault has occurred.
3	VIN_ON/OFF	Disabled because of insufficient input voltage. This could be VIN or VMON.
2	IIN_OC_FAULT	An input overcurrent fault has occurred.
1	IIN_OC_WARN	An input overcurrent warning has occurred.
0	Not Supported	Not supported

11.53 STATUS_TEMPERATURE (7Dh)

Definition: Returns a summary of temperature status.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Command	STATUS_TEMPERATURE (7Dh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit Number	Status Bit Name	Meaning
7	OT_FAULT	An over-temperature fault has occurred.
6	OT_WARN	An over-temperature warning has occurred.
5	Not Supported	Not supported
4	UT_FAULT	An under-temperature fault has occurred.
3:0	Not Supported	Not supported

11.54 STATUS_CML (7Eh)

Definition: Returns a summary of any communications, logic, and/or memory errors.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Command	STATUS_CML (7Eh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit Number	Status Bit Name	Meaning
7	IUCR	Invalid or unsupported PMBus Command was received. This bit sets during device discovery when using PowerNavigator.
6	IUDR	The PMBus command was sent with invalid or unsupported data.
5	PECF	A packet error check failure was detected in the PMBus command.
4	MFD	Memory fault detected. This bit sets if the selected NVM config location is empty or invalid.
3	PFD	Processor fault detected.
2	Not Supported	Not supported
1	OCF	A communication fault other than the ones listed in this table has occurred.
0	OMLF	A memory or logical fault not listed previously was detected.

11.55 STATUS_MFR_SPECIFIC (80h)

Definition: Returns a summary of the manufacturer specific status.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Command	STATUS_MFR_SPECIFIC (80h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit	Status Bit Name	Meaning
7	ADCUNLOCK	ADC clock unlock detected
6	PSYS, IIN Sense	A PSYS and/or sensed I_{IN} OC warning has occurred
5	CFP Fault	A CFP fault has occurred
4	Internal Temperature Fault	The controller internal temp has exceeded 130°C
3	BBEVENT	A black box event occurred
2	LMSEvent	A Last Man Standing event has occurred
1	SPSFault	An SPS overcurrent and/or over-temperature event has occurred
0	SVIDERROR	Error on SVI3 interface

11.56 READ_VIN (88h)

Definition: Returns the input voltage reading. The input source is selected within the LOOPCONFIG command. 10mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: mV

Equation: Read V_{IN} = (Direct value) *10

Command	READ_VIN (88h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two’s Complement Integer															

11.57 READ_IIN (89h)

Definition: Returns the synthesized input current reading. 10mA per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: A

Equation: Read I_{IN} = (Direct value)/100

Command	READ_IIN (89h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.58 READ_VOUT (8Bh)

Definition: Returns the output voltage reading. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: mV

Equation: Read V_{OUT} = (Direct value)

Command	READ_VOUT (8Bh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Unsigned Integer															

11.59 READ_IOUT (8Ch)

Definition: Returns the output current reading. 0.1A per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: A

Equation: Read I_{OUT} = (Direct value)/10

Command	READ_IOUT (8Ch)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.60 READ_TEMPERATURE_1 (8Dh)

Definition: Returns the temperature reading of the hottest power stage per configured rail. 1°C per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: °C

Equation: Read Temperature 1 = (Direct value)

Command	READ_TEMPERATURE_1 (8Dh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.61 READ_TEMPERATURE_2 (8Eh)

Definition: Returns the internal controller temperature reading. 1°C per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: °C

Equation: Read Temperature 2 = (Direct value)

Command	READ_TEMPERATURE_2 (8Eh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.62 READ_POUT (96h)

Definition: Returns the output power. 1W per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: W

Equation: Read P_{OUT} = (Direct value)

Command	READ_POUT (96h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.63 READ_PIN (97h)

Definition: Returns the input power. 1W per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: W

Equation: READ_PIN = (Direct value)

Command	READ_PIN (97h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.64 PMBUS_REVISION (98h)

Definition: Returns the revision of the PMBus specification to which the device is compliant.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: 33h (Part 1 Revision 1.3, Part 2 Revision 1.3)

Command	PMBUS_REVISION (98h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	1	1	0	0	1	1

Bits 7:4	Part 1 Revision	Bits 3:0	Part 2 Revision
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2
0011	1.3	0011	1.3

11.65 MFR_ID (99h)

Definition: Stores inventory information during manufacturing of end products. 4 bytes of space with no defined format.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Default Value: 00000000h

11.66 MFR_MODEL (9Ah)

Definition: Stores inventory information during manufacturing of end products. 4 bytes of space with no defined format.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Default Value: 00000000h

11.67 MFR_REVISION (9Bh)

Definition: Stores inventory information during manufacturing of end products. 4 bytes of space with no defined format.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Default Value: 00000000h

11.68 MFR_DATE (9Dh)

Definition: Stores inventory information during manufacturing of end products. 4 bytes of space with no defined format.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Default Value: 00000000h

11.69 IC_DEVICE_ID (ADh)

Definition: Reports device identification information.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block Read

Default Value: 49D28B00h

Command	IC_DEVICE_ID (ADh)			
Format	Bit Field			
Byte Position	3	2	1	0
Function	MFR Code	ID High Byte	ID Low Byte	Reserved
Default Value	49h	D2h	8Bh	00h

11.70 IC_DEVICE_REV (AEh)

Definition: Reports device revision information.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block Read

Default Value: Based on the revision released

Command	IC_DEVICE_REV (AEh)		
Format	Bit Field		
Bit Position	31:24	23:8	7:0
Function	Hardware Revision	Reserved	Firmware Revision

11.71 DMAFIX (C5h)

Definition: Location for DMA access when performing a fixed address memory access. There is no physical storage for this register.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: 0000h

Units: N/A

11.72 DMASEQ (C6h)

Definition: Location for DMA access when performing a auto-increment address memory access. A series of reads or writes accesses sequential memory locations, with the value of DMAADDR incremented with each access. The reads or writes can be singular 32-Bit transfers or unlimited bursts. There is no physical storage for this register.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: 0000h

Units: N/A

11.73 DMAADDR (C7h)

Definition: Specifies the target address of a DMA read or write to system memory. This command is used for indirect access to any system memory.

Access: Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 00h

Units: N/A

Command	DMAADDR (C7h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field Name	Meaning
15:13	REGION	000 - RAM
12:0	DMAADDR	The 13-Bit target address

11.74 READ_VMON_IINSEN (C8h)

Definition: Returns the input voltage or current reading from the VMON/IINSEN pin depending on configuration. 10mV per LSB for VMON or 10mA per LSB for IINSEN.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: mV or mA depending on configuration

Equation: READ_VMON_IINSEN = (Direct value) * 10

Command	READ_VMON_IINSEN (C8h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.75 BOOTRATE (CCh)

Definition: BOOTRATE sets the slew rate of V_{OUT} during enable and/or disable. TON_RISE must be set to 0 to use BOOTRATE for ramp up, and TOFF_FALL must be set to 0 to use BOOTRATE for ramp down. 10µV/µs per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 01F4h (5000µV/µs)

Units: µV/µs

Equation: BOOTRATE = (Direct value)*10

Range: 10µV/µs to 100000µV/µs

Command	BOOTRATE (CCh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

11.76 PEAK_OC_LIMIT (CDh)

Definition: Sets the peak overcurrent limit thresholds for each phase within a rail. 0.1A per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Equation: Peak Phase OC Limit = (Direct value)/10

Units: A

Default Value: 0258h (60A)

Command	PEAK_OC_LIMIT (CDh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	1	0	1	0	1	1	0	0	0	0

11.77 PEAK_UC_LIMIT (CEh)

Definition: Sets the peak undercurrent limit thresholds for each phase within a rail. 0.1A per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Equation: Peak Phase UC Limit = (Direct value)/10

Units: A

Default Value: FDA8h (-60A)

Command	PEAK_UC_LIMIT (CEh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	1	0	1	0	1	1	0	0	0	0

11.78 VMON_ON (D0h)

Definition: Sets the VMON pin input voltage rising threshold at which the output can be enabled. 10mV per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 01C2h (4500mV)

Units: mV

Equation: VMON On = (Direct value) * 10

Range: 0mV to 32767mV

Command	VMON_ON (D0h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0

11.79 VMON_OFF (D1h)

Definition: Sets the VMON pin input voltage falling threshold at which the output disables. 10mV per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0190h (4000mV)

Units: mV

Equation: VMON_OFF = (Direct value) * 10

Range: 0mV to 32767mV

Command	VMON_OFF (D1h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

11.80 COMPPROP (DDh)

Definition: Sets the proportional gain of the compensation loop.

Access: Paged

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: D90907C4h

Command	COMPPROP (DDh)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Position	Function
31:28	Proportional gain mantissa >8 phase override, use normal P gain if value = 0 and shift = 0
27:25	Proportional gain exponent >8 phase override, use normal P gain if value = 0 and shift = 0
24:21	Proportional gain mantissa 2-phase override, use normal P gain if value = 0 and shift = 0
20	Not Used
19:17	Proportional gain exponent 2-phase override, use normal P gain if value = 0 and shift = 0
16:13	Proportional gain mantissa 1-phase override, use normal P gain if value = 0 and shift = 0
12	Not Used
11:9	Proportional gain exponent 1-phase override, use normal P gain if value = 0 and shift = 0
8	FIR filter length, 0 = none or 1 = ON Must be set if using D term for PID, optional if not using D term
7:4	Proportional gain mantissa is (val/8), all phase counts, if value = 0 gain is 0
3	Not Used
2:0	Proportional gain exponent is 2^(shift-3), all phase counts, if value = 0 and shift = 0 gain is 0

11.81 COMPINTEG (DEh)

Definition: Sets the integral gain of the compensation loop.

Access: Paged

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: 000000A9h

Command	COMPINTEG (DEh)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Position	Function
31:16	Not Used
15:12	Delay time for stepping down gain towards shift. Dcm when in DCM, 0.667µs per gain step
11:8	Gain when in DCM for a while
7:4	Max gain used when Integ movement detected Gain is 2^(-shift-1)
3:0	Gain is 2^(-shift-1)

11.82 COMPDIFF (DFh)

Definition: Sets the differential gain of the compensation loop.

Access: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 0000h

Command	COMPDIFF (DFh)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Setting
15:13	Reserved
12	FIR filter length 0 or 1
11:8	Diff gain mantissa 1-phase override, use normal P gain if value = 0 and shift = 0
7:6	Diff gain exponent 1-phase override, use normal P gain if value = 0 and shift = 0
5:2	Differentiator gain mantissa (val/8)
1:0	Differentiator gain exponent 2^(shift+1 + P-shift) range 0:3

11.83 COMPCFB (E0h)

Definition: Sets the AC current feedback gain of the compensation loop.

Access: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 0560h

Command	COMPCFB (E0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															

Bit Number	Function
15:8	High-pass filter coefficient for current feedback
7:0	Current feedback gain, low droop cases

11.84 HS_BUS_CURRENT_SCALE (E3h)

Definition: Sets the scaling value for the high speed bus output current reporting. 16 bits with 14 fractional bits. A value of 0x4000 is a scale factor of 1.0. A value of 0x0000 is also interpreted as a scale factor of 1.0.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 4000h (1.0)

Units: Scale Factor

Equation: HS Bus Current Scale = (Direct value) * 2^{-14}

Range: 0 to 4.0

Command	HS_BUS_CURRENT_SCALE (E3h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.85 PHASE_CURRENT (E4h)

Definition: Returns the individual phase current reading for the phase selected in PHASE (04h). 0.1A per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: A

Equation: Phase current = (Direct value) / 10

Command	PHASE_CURRENT (E4h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two’s Complement Integer															

11.86 PEAK_OCUC_COUNT (E9h)

Definition: Sets the number of consecutive switch cycles that can exceed the peak per phase overcurrent or undercurrent limit threshold before generating a fault within a rail. A value of 0 disables the fault shutdown and produces a constant current effect.

Access: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Units: Cycles

Default Value: 0606h (6 cycles OC and 6 cycles UC)

Equation: Peak UC Count = (Direct value [15:8]), Peak OC Count = (Direct value [7:0]

Range: 1 cycle to 255 cycles

Command	PEAK_OCUC_COUNT (E9h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Meaning
15:8	Number of consecutive switch cycles exceeding peak UC limit before fault
7:0	Number of consecutive switch cycles exceeding peak OC limit before fault

11.87 SLOW_IOUT_OC_LIMIT (EAh)

Definition: Sets the slow sum output overcurrent fault threshold. 100mA per LSB. A value of 0 disables this function.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 00C8h (20A)

Units: A

Equation: Slow I_{OUT} OC Limit = (Direct value) / 10

Range: 1A to 3276A

Command	SLOW_IOUT_OC_LIMIT (EAh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.88 FAST_OC_FILT_COUNT (EBh)

Definition: Sets the fast sum output overcurrent fault filter settings.

Access: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 0696h (Filter = 10.6µs, Delay = 100µs)

Command	FAST_OC_FILT_COUNT (EBh)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Purpose	Setting
15:12	Not Used	Not used
11:8	Filter Setting	Time constant = 166.7ns*2^direct value. Range is 167ns to 5.46ms.
7:0	Delay Setting	Delay 0.667µs* direct value before a fault is generated. Range is 0µs to 170µs.

11.89 SLOW_OC_FILT_COUNT (ECh)

Definition: Sets the slow sum output overcurrent fault filter settings.

Access: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 0606h (Filter = 10.6µs, Delay = 1,024µs)

Command	SLOW_OC_FILT_COUNT (ECh)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0

Bit Number	Purpose	Setting
15:12	Not Used	Not Used
11:8	Filter Setting	Time constant = 166.7ns*2^direct value. Range is 167ns to 5.46ms.
7:0	Delay Setting	Delay 170.7µs* direct value before a fault is generated. Range is 0µs to 43.5ms.

11.90 LOOPCFG (F0h)

Definition: Configures various rail settings. To make a change, read the value, modify only the desired bits, and write the value while preserving the reserved bit settings.

Access: Paged

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: 102071F6h

Command	LOOPCFG (F0h)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Position	Field	Function
31	Not Used	Not used
30:29	Reserved	Reserved
28	Diode Emulation Mode	1 = Enable diode emulation for PS0/1
27:12	Reserved	Reserved
11:8	Minimum Phase Count	Minimum phase count, 0-11
7	Reserved	Reserved
6	Diode Emulation Enable	1 = Enable diode emulation
5:4	Lock SVID	PMBus overrides of SVID: 0 = Reject, 1 = Offset, 2 = +power state, 3 = +voltage
3:1	Reserved	Reserved
0	APD enable	1 = Enable auto phase add/drop

11.91 RESTORE_CFG (F2h)

Definition: Identifies the user configuration ID to be restored from NVM and loads the store's settings into the device active memory. This command should only be used while all outputs are disabled. Restore takes 3ms to complete.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

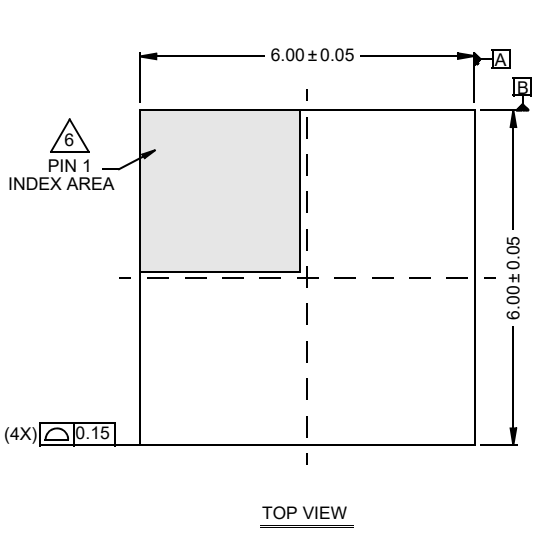
Default Value: 00h

Command	RESTORE_CFG (F2h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

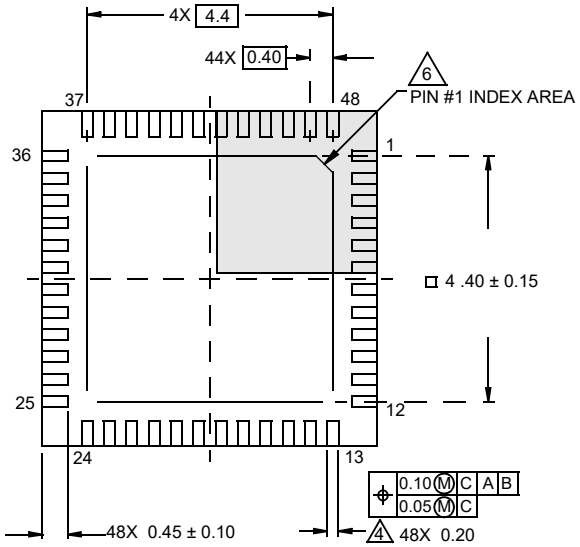
Bit Number	Status Bit Name	Meaning
7:4	Reserved	Reserved
3:0	CONFIG	Selected user configuration ID to restore, 0-15.

12. Package Outline Drawing

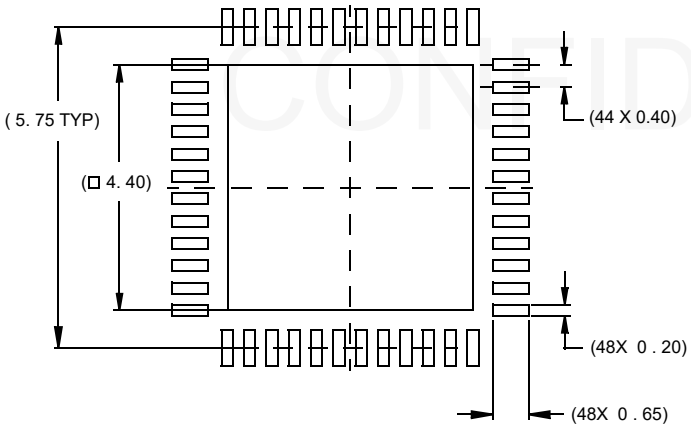
L48.6X6
48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 7/14



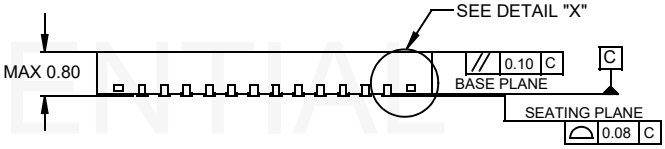
TOP VIEW



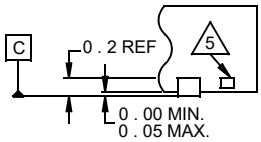
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

13. Ordering Information

Part Number[1][2]	Part Marking	Junction Temperature (°C)	Tape and Reel (Units)[3]	Package (RoHS Compliant)	Pkg. Dwg. #
RAA229620GNP#AA0	RAA229620	-40 to +125	-	48 Ld 6x6 QFN	L48.6x6
RAA229620GNP#HA0	RAA229620	-40 to +125	4k	48 Ld 6x6 QFN	L48.6x6
RAA229620GNP#MA0	RAA229620	-40 to +125	250	48 Ld 6x6 QFN	L48.6x6

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA229620 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

Table 4. Power Stage Recommendations

Part Number	Rating (A)	Type	TOUT	TREF	REFIN	FAULT#	Package Dwg. #	Pin-to-Pin Compatible	Typically Used With
5.0V PWM Power Stage Family									
ISL99360B	60	SPS	Yes	No	Yes	Yes	L32.5x5W	N/A	5V PWM Inputs, Phase Doublers Required: ISL6617A
ISL99380B	80	SPS	Yes	No	Yes	No	L39.5x6A	N/A	
3.3V PWM Power Stage Family									
ISL99360	60	SPS	Yes	No	Yes	Yes	L32.5x5W	N/A	Full Digital Controllers: ISL68/69xxx
ISL99380	80	SPS	Yes	No	Yes	No	L39.5x6A	ISL99390	
ISL99390	90	SPS	Yes	No	Yes	No	L39.5x6A	ISL99380	

14. Revision History

Rev.	Date	Description
0.3	May 13, 2021	Updated DAC (VID + Offset) section in EC table. Applied new template.
0.2	Oct.8.20	Added VMON function back in.
0.1	Aug.4.20	Updated the System Accuracy specifications in the EC table.
0.0	Jul.14.20	Initial Preliminary release

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(Rev.1.0 Mar 2020)

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