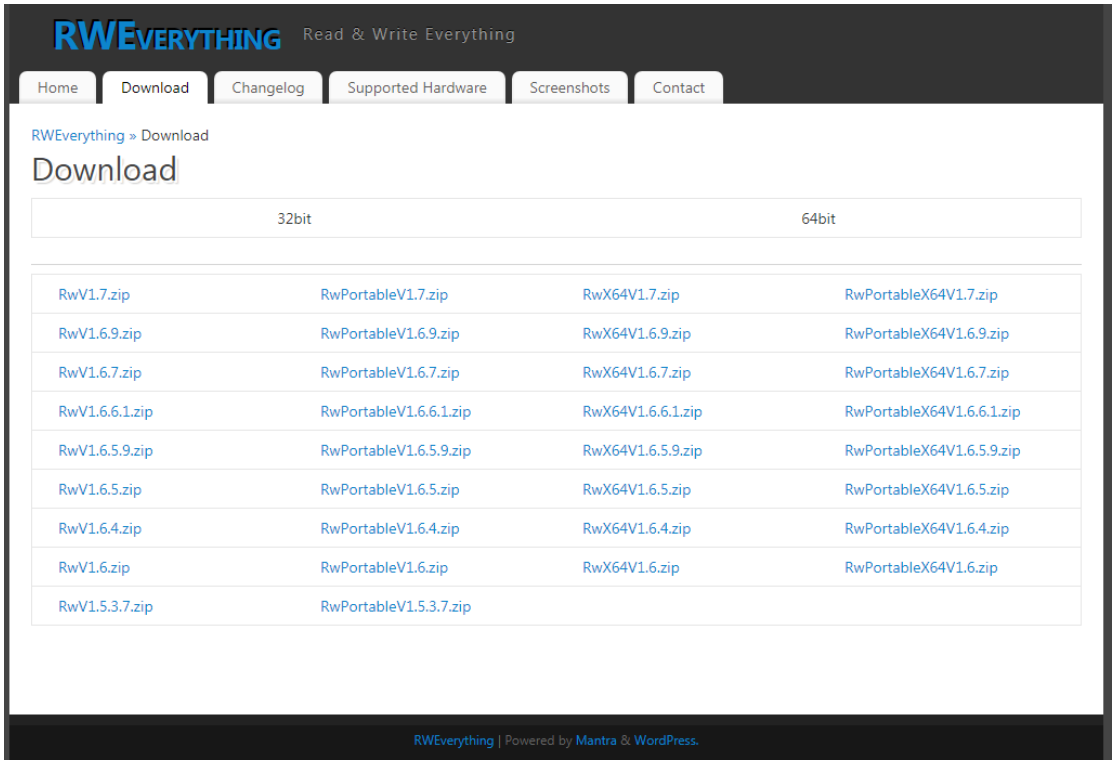
ASRockRack Technical Document

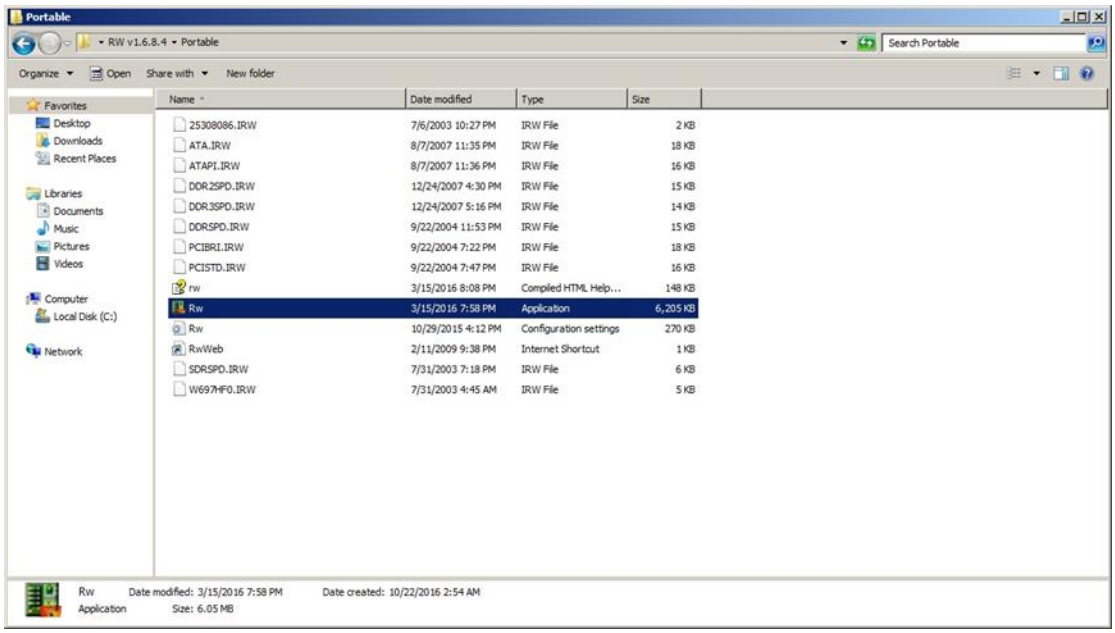
How to check Nvdimm disable patch SOP ver.1.0

1. Download Tool “RW” from website link below:

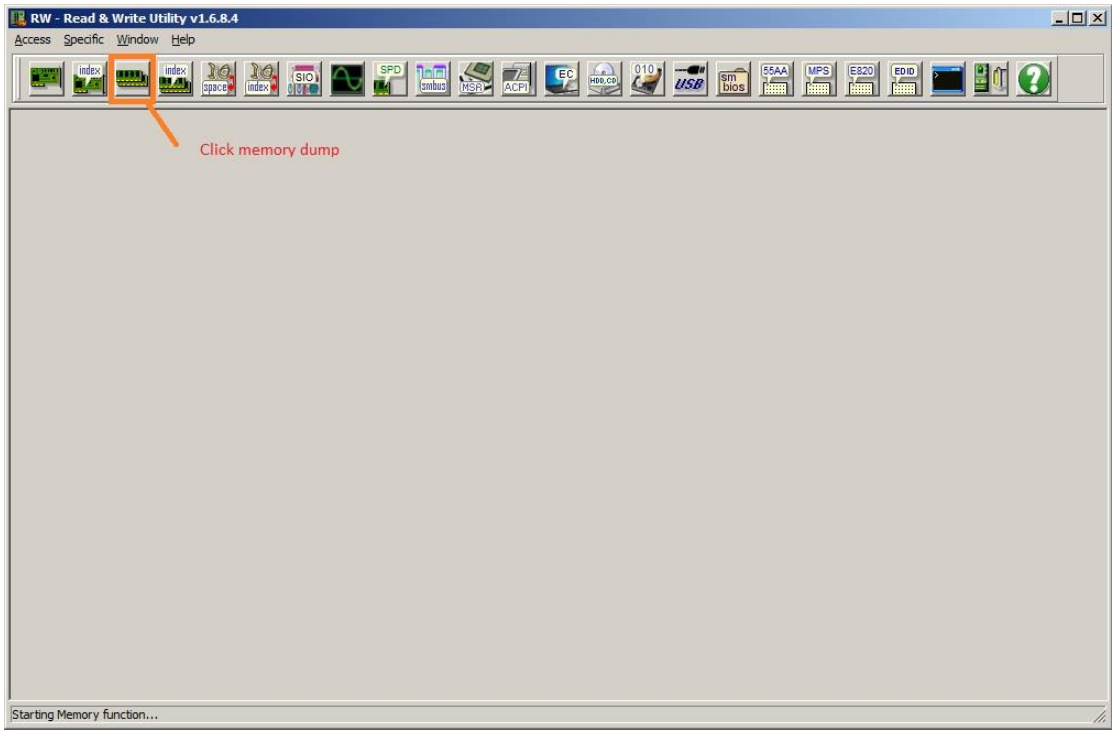
https://rweverything.com/download/



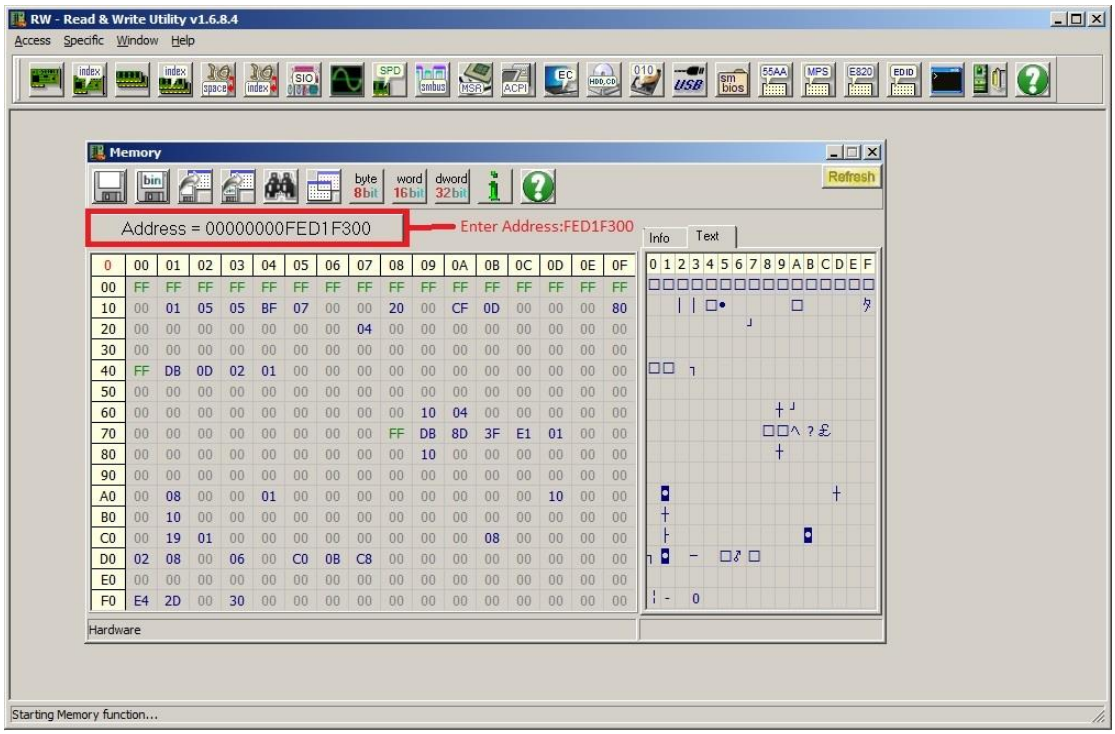
2. Boot to Windows, and execute “RW”



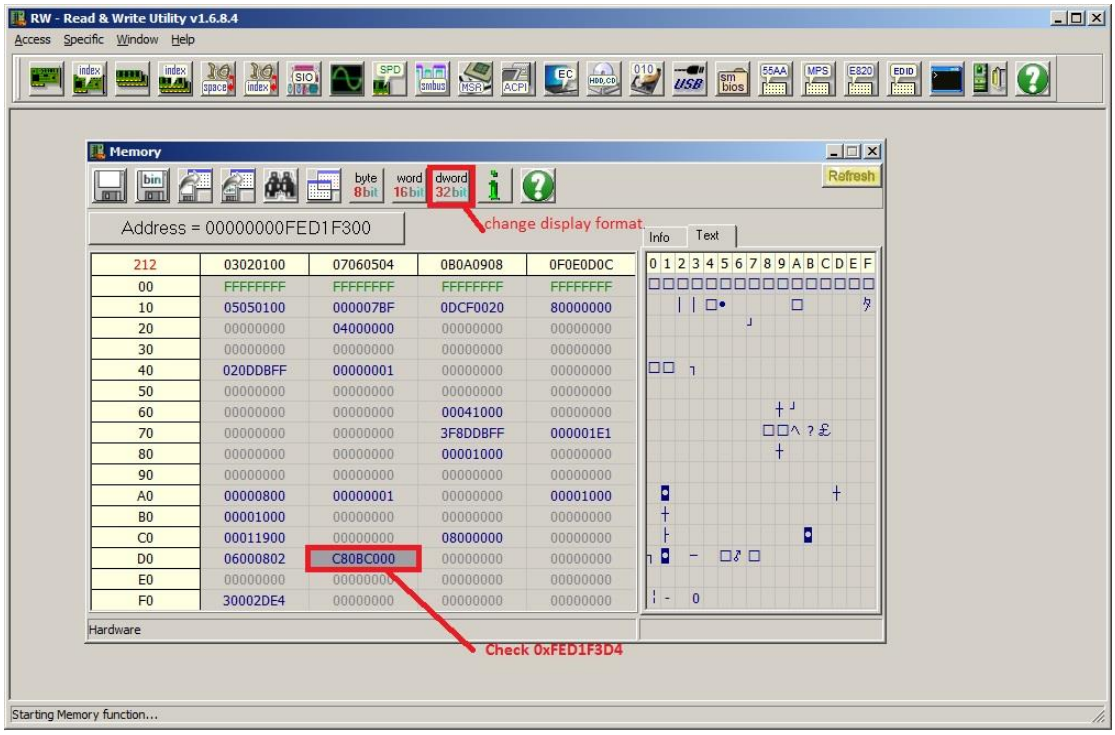
3.Execute “check memory dump” buttom



4.Setup Memory Address: **0xFED1F300**

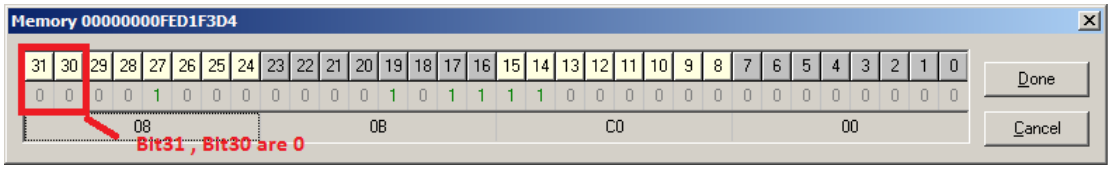


5. Change display format to dword type, and check register 0xD4.



6. Check Bit30 and Bit31:

If Bit 30 and Bit 31 are 0, Nvdimm disable patch is correct.



Appendix

This Nvdimm disable patch check SOP is based on reference documents below:

Intel Document Number: 511555, Revision: 2.1

10.1.80 CIR33D4—Chipset Initialization Register 33D4

10.1.80 CIR33D4 — Chipset Initialization Register 33D4

Offset Address: 33D4–33D7h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31	**GPIO_D to PM_SYNC Enable (GPIO_D_PM_SYNC_EN)** — R/W. 0 = GPIO_D (as selected in RCBA+33C8h) pin state not sent to processor over PMSYNC. 1 = GPIO_D state sent to processor over PMSYNC.
30	**GPIO_C to PM_SYNC Enable (GPIO_C_PM_SYNC_EN)** — R/W. 0 = GPIO_C (as selected in) pin state not sent to processor over PMSYNC. 1 = GPIO_C state sent to processor over PMSYNC.
29	**GPIO_B to PM_SYNC Enable (GPIO_B_PM_SYNC_EN)** — R/W. 0 = GPIO_B (as selected in) pin state not sent to processor over PMSYNC. 1 = GPIO_B state sent to processor over PMSYNC.
28	**GPIO_A to PM_SYNC Enable (GPIO_A_PM_SYNC_EN)** — R/W. 0 = GPIO_A (as selected in) pin state not sent to processor over PMSYNC. 1 = GPIO_A state sent to processor over PMSYNC.
27:0	**CIR33D4 Field 1** — R/W. BIOS must program this field to 0x80BC000.

Change GPIO_C (Bit30) and GPIO_D (Bit31) from 1 to 0.

RCBA Base Address value

12.1.40 RCBA—Root Complex Base Address Register (LPC I/F—D31:F0)

Offset Address: F0–F3h Attribute: R/W
Default Value: 00000000h Size: 32 bit

Bit	Description
31:14	**Base Address (BA)** — R/W. Base Address for the root complex register block decode range. This address is aligned on a 16-KB boundary. This gets locked when ULKMC.RCBALK=1. BIOS must configure the BA prior to setting RCBALK.
13:1	Reserved
0	**Enable (EN)** — R/W. When set, this bit enables the range specified in BA to be claimed as the Root Complex Register Block.