



ASRockRack Technical Document

How to check Nvdimmm disable patch SOP ver.1.0

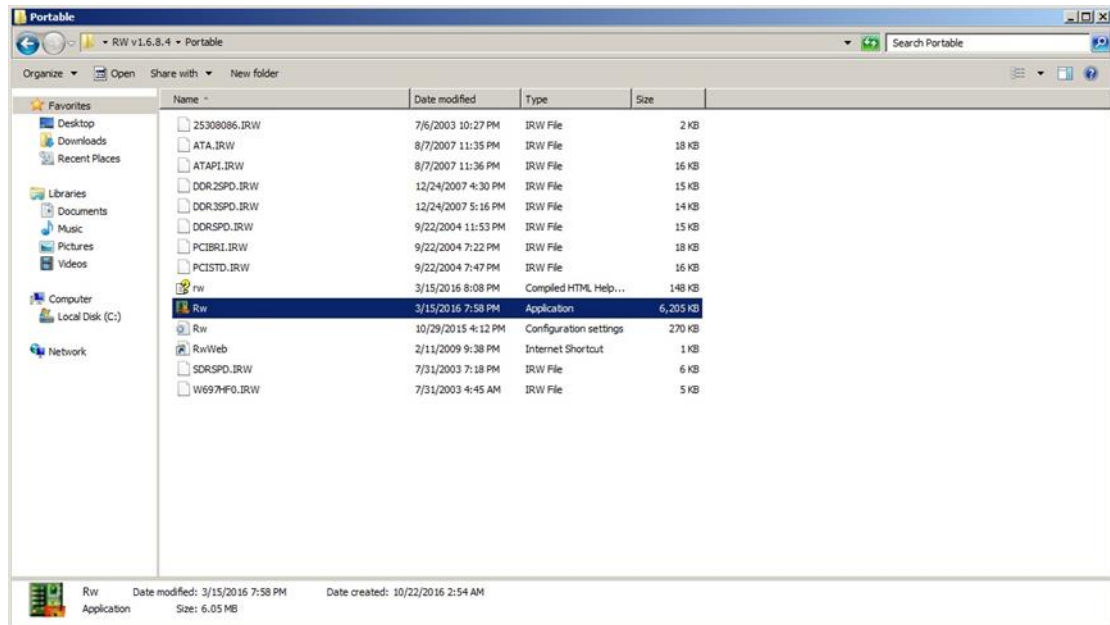
1. Download Tool "RW" from website link below:

<https://rweverything.com/download/>

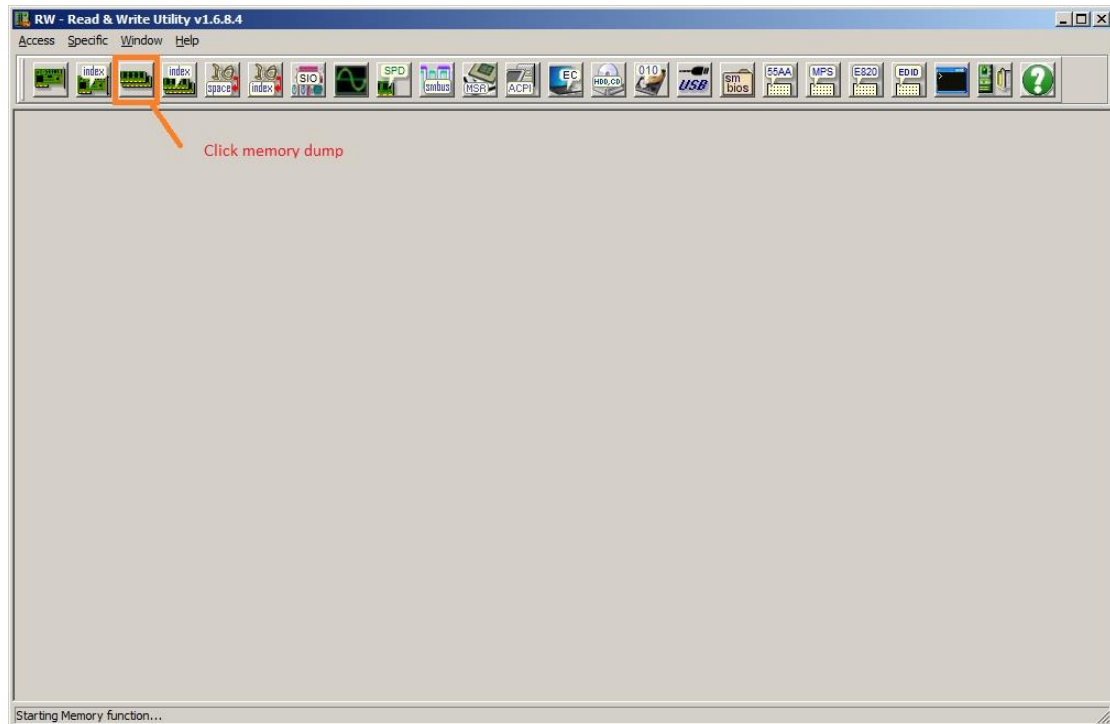
A screenshot of the RWEVERYTHING website's download page. The page has a dark header with the logo and tagline "Read & Write Everything". Below the header is a navigation menu with buttons for Home, Download, Changelog, Supported Hardware, Screenshots, and Contact. The main content area shows the breadcrumb "RWEverything » Download" and the heading "Download". There are two tabs for "32bit" and "64bit". A table lists various software versions for download, including standard, portable, and X64V versions for different releases.

32bit		64bit	
RwV1.7.zip	RwPortableV1.7.zip	RwX64V1.7.zip	RwPortableX64V1.7.zip
RwV1.6.9.zip	RwPortableV1.6.9.zip	RwX64V1.6.9.zip	RwPortableX64V1.6.9.zip
RwV1.6.7.zip	RwPortableV1.6.7.zip	RwX64V1.6.7.zip	RwPortableX64V1.6.7.zip
RwV1.6.6.1.zip	RwPortableV1.6.6.1.zip	RwX64V1.6.6.1.zip	RwPortableX64V1.6.6.1.zip
RwV1.6.5.9.zip	RwPortableV1.6.5.9.zip	RwX64V1.6.5.9.zip	RwPortableX64V1.6.5.9.zip
RwV1.6.5.zip	RwPortableV1.6.5.zip	RwX64V1.6.5.zip	RwPortableX64V1.6.5.zip
RwV1.6.4.zip	RwPortableV1.6.4.zip	RwX64V1.6.4.zip	RwPortableX64V1.6.4.zip
RwV1.6.zip	RwPortableV1.6.zip	RwX64V1.6.zip	RwPortableX64V1.6.zip
RwV1.5.3.7.zip	RwPortableV1.5.3.7.zip		

2. Boot to Windows, and execute "RW"



3. Execute "check memory dump" button



Appendix

This Nvdimm disable patch check SOP is based on reference documents below:

Intel Document Number: 511555, Revision: 2.1

10.1.80 CIR33D4—Chipset Initialization Register 33D4

10.1.80 CIR33D4 — Chipset Initialization Register 33D4

Offset Address: 33D4–33D7h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31	GPIO_D to PM_SYNC Enable (GPIO_D_PM_SYNC_EN) — R/W. 0 = GPIO_D (as selected in RCBA+33C8h) pin state not sent to processor over PMSYNC. 1 = GPIO_D state sent to processor over PMSYNC.
30	GPIO_C to PM_SYNC Enable (GPIO_C_PM_SYNC_EN) — R/W. 0 = GPIO_C (as selected in) pin state not sent to processor over PMSYNC. 1 = GPIO_C state sent to processor over PMSYNC.
29	GPIO_B to PM_SYNC Enable (GPIO_B_PM_SYNC_EN) — R/W. 0 = GPIO_B (as selected in) pin state not sent to processor over PMSYNC. 1 = GPIO_B state sent to processor over PMSYNC.
28	GPIO_A to PM_SYNC Enable (GPIO_A_PM_SYNC_EN) — R/W. 0 = GPIO_A (as selected in) pin state not sent to processor over PMSYNC. 1 = GPIO_A state sent to processor over PMSYNC.
27:0	CIR33D4 Field 1 — R/W. BIOS must program this field to 0x80BC00.

Change GPIO_C (Bit30) and GPIO_D (Bit31) from 1 to 0.

RCBA Base Address value

12.1.40 RCBA—Root Complex Base Address Register (LPC I/F—D31:F0)

Offset Address: F0–F3h Attribute: R/W
Default Value: 00000000h Size: 32 bit

Bit	Description
31:14	Base Address (BA) — R/W. Base Address for the root complex register block decode range. This address is aligned on a 16-KB boundary. This gets locked when ULKMC.RCBALK=1. BIOS must configure the BA prior to setting RCBALK.
13:1	Reserved
0	Enable (EN) — R/W. When set, this bit enables the range specified in BA to be claimed as the Root Complex Register Block.